CHAPTER 1

Metal Oxide Semiconductor Field Effect Transistors

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PART ONE: BASICS OF METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS

The **metal oxide semiconductor field effect transistor** (**MOSFET**) is the most basic element of integrated circuits (IC) which is used in many electrical devices in our daily life. The transistor has four-terminal contacts: gate (G), source (S), drain (D), and substrate body (B). In a transistor, the body terminal can be connected to the source to make it a three-terminal device. MOSFETs have different symbols depending on the operating mode and type of dopant in the channel as shown in Figure 1.1. The drive carriers in nMOS is electrons (n-channel) but the body is p-type doped meanwhile pMOS the main carriers are holes (p-channel) with n-type doped body

In principle, MOSFET structure consists of two PN junctions (SB and DB regions) and carrier transport occurs in channel region between source and drain. The SB and DB PN junctions are connected back-to-back and this prevents the current flow in the channel. By applying a voltage to the gate contact, an electric field is established through the oxide and the transistor can be turned on or off. MOSFETs can be used as switch or amplifier in the circuits.

In case of a switch, the resistance R_{DS} is dependent on V_{GS} ($R_{DS} = f(V_{GS})$). The transistor is in on-state when a large on-state current (I_{on} is high) flows and it is off when a very small off-state leakage current is obtained (I_{off} is low). A MOSFET acts as an amplifier when $I_D = f(V_{GS})$ or the drain current is voltage-controlled.

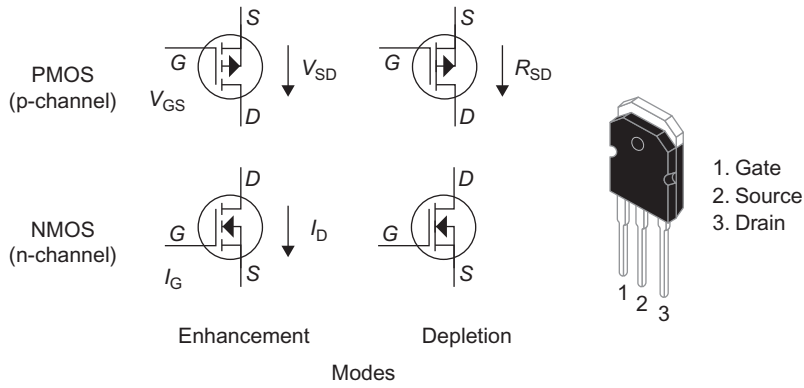

Figure 1.1 FET's symbols with related voltages (V_{SD} and V_{GS}), currents (I_D and I_G), and resistance (R_{SD}).

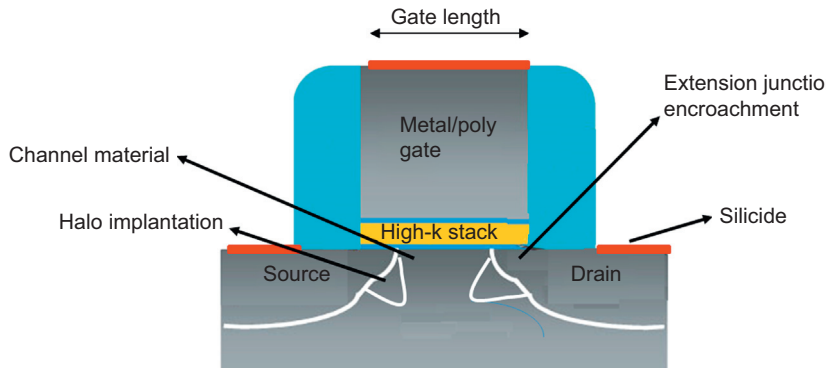

Figure 1.2 A schematic of MOSFET structure.

MOSFETs are manufactured in 2D or 3D designs on silicon bulk or silicon on insulator (SOI) substrates. The traditional MOSFET source/drain (S/D) junctions and the extended junctions are formed by implantation. A tilted angle implantation is also used to further adjust the doping profile below the gate region (so-called Halo implantation). Stressor materials such as silicon−germanium, carbon-doped silicon, or germanium−tin may induce strain in the channel region to enhance the carrier mobility. Nitride layers which are deposited over the transistor structure are also used as stressor materials. The channel material is Si, but other novel materials such as germanium, germanium−tin, III−V materials, graphene, and graphene-like materials have been used too. The dielectric material was for a long time SiO_2 (until 90 nm node) which later replaced by high-*k* materials to avoid the leakage of thin oxide layers. In order to decrease the contact resistances in the transistors silicide layers were formed prior to meatllization. Figure 1.2 shows a 2D MOSFET structure

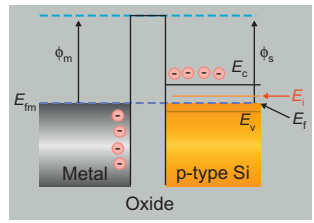

Figure 1.3 Energy band diagram for metal–oxide–semiconductor.

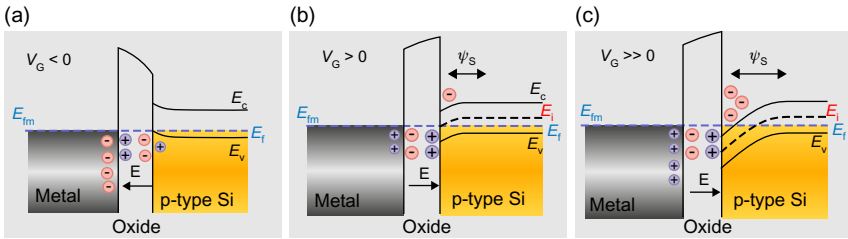

Figure 1.4 (a) Accumulation, (b) depletion, and (c) inversion operation modes for a MOSFET. The mid band-gap and fermi levels are marked by E_i *(in red) and* E_f *(in blue).*

where different parts of a transistor are indicated. Sidewall transfer lithography (STL) technique has been widely used to manufacture MOSFETs in down to 14 nm node.

SURFACE SPACE–CHARGE REGIONS IN MOSFETs

The MOSFET structure has three main parts: metal, oxide, and semiconductor. Initially, the Fermi level is aligned and the energy bands are flat and the workfunctions are the same for all three parts as shown in Figure 1.3. In this situation, there is no charge neither inside the oxide nor at the interface between the oxide and semiconductor.

Applying a voltage to the gate electrode causes an electric field E between the both sides. This makes a displacement of carriers near each side forming a two space–charge region.

When no charge is present at the interface between the oxide and semiconductor, the flatband voltage (V_{FB}) is described as difference between the gate metal workfunction (φ_M) and the semiconductor workfunction, ϕ_S: $V_{FB} = \varphi_M + \phi_S$.

The charge density in the semiconductor (channel region) is dependent on the applied voltage to the metal (or poly) gate. Figure 1.4(a)–(c) shows three conditions for an nMOSFET that can occur when a voltage is applied to the gate terminal: accumulation, depletion, and inversion.

An nMOSFET is in on-state when a negative voltage is applied to the gate and the conductivity of Si channel is increased. The negative voltage (φ_s) results in a bending of the energy bands upward (E_f is constant). The modified energy band makes more holes accumulated in channel region as shown in Figure 1.4(a). In this case, the gate voltage is distributed across the oxide layer and the formed voltage in semiconductor is given by $V_{GS} = V_{ox} + \psi_{Si}$.

In general, the density of accumulated carriers at the surface for a biased gate can be obtained as the following:

$$n = n_i e^{\frac{(E_f - E_i)}{kT}} \tag{1.1a}$$

$$p = p_i e^{\frac{(E_i - E_f)}{kT}} \tag{1.1b}$$

where E_i is the mid-gap energy in the bandgap. More carriers will be available when the band-bending increases. These equations show that for the carrier accumulation condition in an nMOSFET, p > n when $E_i - E_f$ becomes large (holes in the channel region).

The carrier condition changes when a small or moderate positive voltage is applied to the gate. This is known as carrier depletion for the transistors and at this time the energy bands bend downward as shown in Figure 1.4(b). The value of $E_i - E_f$ decreases and the channel region is now depleted of holes. The total charge in the established space–charge region in semiconductor with the depletion width (t_d) is obtained from the equation

$$Q_s = q\, N_s\, t_d \tag{1.2}$$

where N_s is the dopant concentration in the semiconductor. The negative sign is due to the polarity of the charge in the depletion region. The depletion length in the semiconductor is obtained by solving the Poisson equation. Therefore, the formed electric field, ξ_s in semiconductor's depletion region can be written as

$$\frac{d\xi}{dx} = \frac{qN_s}{K_s \varepsilon_0} \quad (0 < x < t_d) \Rightarrow \xi(x) = \frac{qN_s}{K_\varepsilon \varepsilon_o}(t_d - x) \tag{1.3}$$

where K_s is dielectric constant of semiconductor and ε_0 is permittivity. The electric field in Eq. (1.3) is defined in terms of the raised electrostatic potential as $\xi(x) = -\mathrm{d}\psi_s/\mathrm{d}x$ and after integration, the potential change is written as:

$$\psi_s(t_d) - \psi_s(x) = \frac{qN_s}{2K_\varepsilon\varepsilon_0}(t_d - x)^2 \tag{1.4}$$

In case of $x = 0$, the potential denoted by $\psi_s$has the following relationship with the depletion width:

$$\psi_s = \frac{qN_s t_d^2}{2K_s\varepsilon_0} \tag{1.5}$$

If a relatively large positive voltage is applied to the gate electrode, then the band-bending downward becomes severe. This condition may cause the mid-gap energy E_i to pass E_f near the Si and oxide interface. As a consequence, an inversion layer is established where the electrons will have greater density than holes. A strong inversion layer is desired for MOSFETs operation, as shown in Figure 1.4(c). When the density of electrons becomes equal the to the hole density in the bulk, a moderate inversion has been achieved.

Threshold voltage (V_T) is a critical voltage for MOSFETs and it refers to the situation when the applied gate voltage (V_{GS}) is reached to a value resulting in a significant extended inversion layer and rapid inverse charge. Thus the voltages can be written from flatband voltage equation as

$$V_T = -\frac{Q}{C_0} + \phi_{Si} \quad \text{where} \quad C_0 = \frac{K_0\varepsilon_0}{x_0} \tag{1.6a}$$

We notify here that a band bending occurs in the Si side due to workfunction differences between the Si and metal, charges in oxide and surface states.

Then, the threshold voltage is modified to:

$$V_T = V_{FB} + \phi_{Si} - \frac{Q_s}{C_0} \tag{1.6b}$$

where φ_{Si} is the workfunction of Si. In eq. (1.6b), Q_s under strong inversion can be obtained from $Q_s = -\sqrt{2qK_s\varepsilon_0 N_a(\psi_s + \varphi_{Si})}$ where ψ_s is the voltage of the n-inversion side of the junction where Si is p-type doped.

LEAKAGE COMPONENTS IN MOSFETs

There are different leakage components in MOSFETs depending on the transistor size: subthreshold leakage current, gate−oxide leakage, and junction leakage.

These leakage sources have become more important due to the continuous downscaling of transistors. The supply voltage is being decreased to reduce both dynamic power consumption and electric fields inside the transistor structure. All leakage sources in a transistor manufactured in a technology generation may cause in the dissipation of a large amount of power.

SUBTHRESHOLD CURRENT

From the definition of threshold voltage, it is concluded that the inversion layer charge is zero below this voltage. But in fact, there is a subthreshold current which decreases exponentially by gate voltage decrease below the threshold voltage as shown in Figure 1.5.

The amount of subthreshold drive current is regulated by the threshold voltage which lies between ground and the supply voltage. The gate voltage is expressed in terms of semiconductor potential and flatband voltage as the following:

$$V_G = V_{FB} + \psi_s + V_o = V_{FB} + \psi_s + \frac{\sqrt{2q\varepsilon_s\psi_s}}{C_0} \tag{1.7}$$

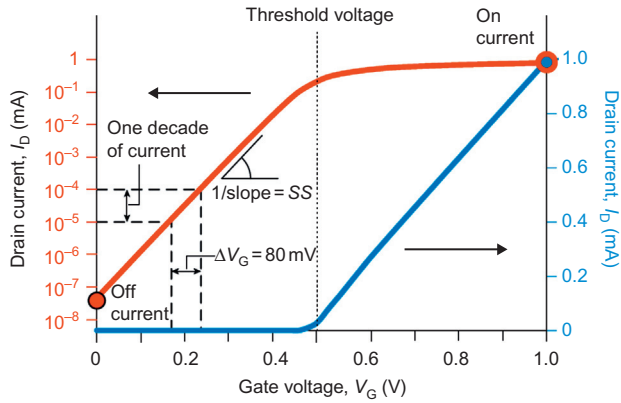

Figure 1.5 I (V) curve of a MOSFET when the gate voltage of typically 1 V is applied. The subthreshold voltage is estimated to 80 mV in the figure [1].

The variation of the gate voltage in terms of semiconductor potential is expressed as

$$\frac{dV_G}{d\psi_s} = 1 + \frac{1}{2C_0}\sqrt{\frac{q\varepsilon_s}{\psi_s}} \approx 1 + \frac{1}{2C_0}\sqrt{\frac{q\varepsilon_s}{2\phi_f}} = n \tag{1.8}$$

where the semiconductor potential is estimated to be $2\phi_f$ for threshold. Then, subthreshold current is obtained from

$$I_D \propto Q \propto \exp\left(\frac{\psi_s}{V_T}\right) \propto \exp\left(\frac{V_G}{nV_T}\right) \tag{1.9}$$

GATE–OXIDE LEAKAGE

The oxide breakdown and oxide reliability are issues arisen by downscaling of the MOSFETs. The tunneling of carriers through the oxide is enhanced when its thickness is shrunk. The carriers gradually damage the oxide layer which is known as time-dependent destructive breakdown (TDDB). High-k materials with large dielectric constant may solve this problem. Typically HfO, Al_2O_3, and ZrO dielectrics have been integrated in MOSFETs [2]. A wider overlook of high-k materials is provided in Chapter 4.

S/D JUNCTION LEAKAGE

Both source-to-substrate and drain-to-substrate junctions can affect many transistor characteristics: the current–voltage characteristics, lowering output resistance, and the speed of transistor. The junction leakage has influence on the standby power dissipation.

Due to downscaling of MOSFETs, the junctions are designed for higher doping levels (halo doping is applied) and shallower depths. Heavier doping in source and drain results in thinner depletion layers and more recombination centers. An annealing step is applied to remove the lattice damage after junction dopant implantation, which can further increase the junction leakage.

MOS CAPACITORS

The MOS structures in Figure 1.3 are basically capacitors with the oxide (SiO_2 or high-k oxide) as dielectric material. The capacitances of space–charge layer in Si (C_s) and oxide (C_{ox}) with thickness of x_0 are in series and are defined as

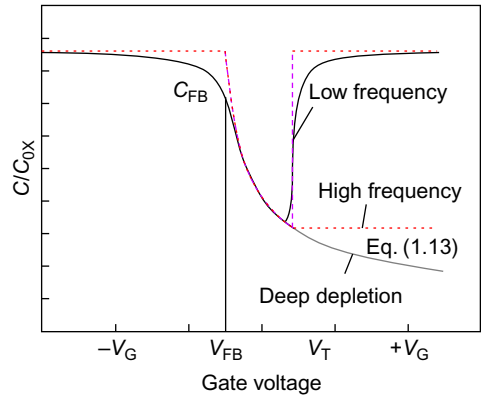

Figure 1.6 C–V characteristic for low and high frequencies [3].

$$C_s = \frac{K_s \varepsilon_0}{x_d} \tag{1.10a}$$

$$C_{ox} = \frac{K_s \varepsilon_0}{x_0} \tag{1.10b}$$

The gate voltage is expressed as

$$V_G = -\frac{Q_s}{C_s} + \psi_s \tag{1.11}$$

Then the depletion thickness will be

$$t_d = \frac{K_s \varepsilon_0}{C_{ox}} \left(\sqrt{1 + \frac{2 V_G C_{ox}^2}{q K_s \varepsilon_0 N_a}} - 1 \right) \tag{1.12}$$

The total capacitance, C ($C = C_s\ C_{0x}/(C_s + C_{0x})$) for MOS structure is easily obtained from the following equation (as shown in Figure 1.6):

$$C = \frac{C_{ox}}{\sqrt{1 + (2C_{ox}^2/qN_a K_s \varepsilon_0) V_G}} \tag{1.13}$$

STATIC CHARACTERIZATION OF MOSFETs

In order to discuss the I–V characteristics of MOSFETs, different parameters have to be defined:

Threshold voltage (V_T).
Voltages between D and S terminals (V_{DS}) and between G and S terminals (V_{GS}).

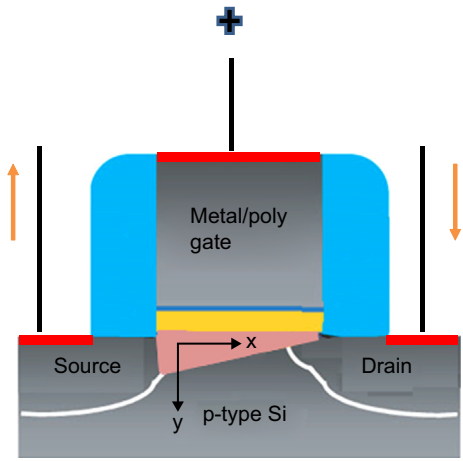

Figure 1.7 A schematic of a biased nMOSFET. The marked triangle shows the formed potential in the channel region.

Supply voltage (V_{DD}).
Overdrive voltage (V_{ov}): when V_{GS} exceeds the threshold. V_{OV} is defined as $V_{GS} - V_T$.
Channel length and width, L and w (aspect ratio: L/W).
Oxide capacitance (C_{ox}).
Channel mobility (μ_e).

Coefficient of conductance (k_n) is defined as $k_n = \mu_e C_{ox}(W/L)$

A schematic of an nMOSFET structure is shown in Figure 1.7. When no voltage is applied to the gate terminal, the conductance in the channel is low and no current flows between source and drain terminals ($I_D = 0$). This situation changes rapidly if a positive voltage is applied to the gate. In order to have a large enough conductance in the channel so that the electrons flow, the gate applied voltage has to be greater than the threshold voltage ($V_{GS} > V_T$).

Upon flow of current between source and drain terminals with assumption of $V_{GS} > V_T$, a graded voltage forms across the channel region as shown in Figure 1.8. It is important that $V_{DS} < V_{GS} - V_T$, otherwise a pinch through situation may occur.

In this case, V_{GS} will control the conductance of the channel or, in other words, the channel acts as a variable resistor. Thus, the

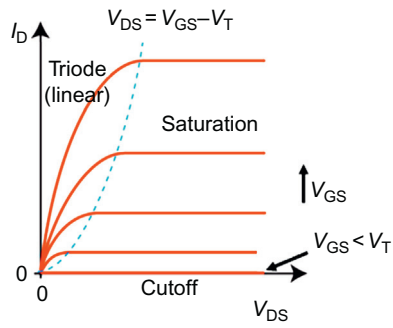

Figure 1.8 IV characteristics of an n-channel MOSFET in different operation modes [3].

conductance between source and drain (g_{DS}) is dependent on both V_{GS} and V_{DS}. The g_{DS} is obtained from this expression:

$$g_{DS} = \frac{1}{r_{DS}} = k_n\left(V_{GS} - V_t - \frac{1}{2}V_{DS}\right) \tag{1.14}$$

where r_{DS} is the resistance between source/drain.

The induced channel charge is written as the following: $Q_I = -C_{ox}(V_G - V_T - \psi)$.

Therefore, the channel current can also be calculated by carrier mobility, the formed electric field along the channel direction, channel length, and channel charge according to

$$I_D = W\mu_n Q_I \xi_y \tag{1.15}$$

where the formed electric field along the channel direction is given by: $\xi_y = -d\psi/dy$

Therefore, I_D relationship can be rewritten as

$$I_D\, dy = W\mu_n C_{ox}(V_{GS} - V_T - \psi)d\psi \Rightarrow$$

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{1.16a}$$

Then, the expression may be rephrased using coefficient of conductance as

$$I_D = k_n\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{1.16b}$$

The I_D expression is a quadratic function of V_{DS} with a maximum point at V_T. Expression 1.15 is very important for transistor characterization and is applied to derive the channel mobility from the electrical measurements.

An nMOSFET will have three modes with the following condition as shown in Figure 1.8:

1. Cutoff: when $V_{GS} < V_T$ and the channel current $I_D = 0$ A.
2. Triode or linear mode if $0 < V_{DS} < V_{GS} - V_T$ conductance is high for the carriers to flow along the channel with a current of I_D. There are two electrical fields along x- and y-directions that are marked in Figure 1.7. The electrical field along y generates the inversion layer, whereas the field along x-direction causes the carriers move along the channel direction.
3. Saturation mode when $V_{DS} \geq V_{GS} - V_T$. This is a voltage-controlled current source (VCCS). The drain current can be rewritten as $I_D = (1/2)k_n(V_{GS} - V_T)^2$. So far, the characteristics of nMOS have been discussed but for pMOS all currents and voltages and voltages conditions will be reversed. This means that V_T, V_{SG}, V_{DS} and V_{OV} will be negative and for example, conditions for saturation mode $V_{GS} < V_T$ and $V_{DS} < V_{OV}$.

The MOSFET operates as a switch when it shifts between linear and cutoff modes. The transistor may act as an amplifier in the circuit as shown in Figure 1.9.

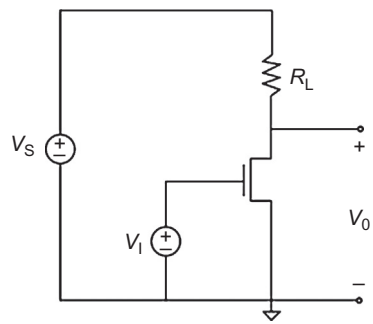

Figure 1.9 An nMOS transistor in a circuit acting as an amplifier.

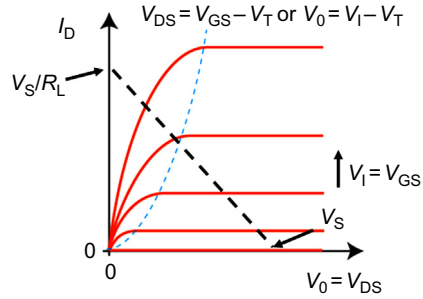

Figure 1.10 IV characteristics of an nMOSFET designed as an amplifier.

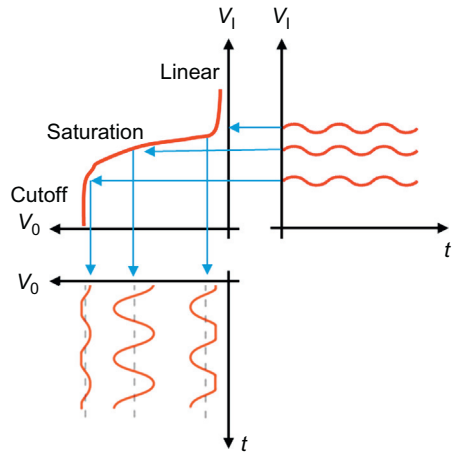

Figure 1.11 Signals to n-channel MOSFET in different operation modes.

In this simple circuit, R_L may act as a load resistance to the transistor. The transistor acts as an amplifier at the intersections of load line with the MOSFET characteristic curves as shown in Figure 1.10.

When a signal is delivered to a MOSFET, the outcome can be illustrated for different modes as shown in Figure 1.11.

TRANSFER FROM 2D TO 3D NANOSCALED TRANSISTORS

Over four decades, MOSFET was manufactured in 2D structure until a nonplanar 3D transistor was introduced in the form of a fin field effect transistor (FinFET) processed on SOI substrates. The term FinFET was introduced by University of California [4]. FinFETs have entirely different design and characteristics than the planar transistors. The

distinctive characteristic of a FinFET is that the body of the device is a thin fin of Si where its thickness is the effective channel length of the transistor. Therefore, all categories of these transistors are also known as multigate FETs (MUGFETs). In general, most of the MUGFETs have a number of parallel nanowires (the so-called fingers) which have a joint gate electrode. This structure permits the current drive to be enlarged by increasing the number of fingers of the transistor.

A benefit of 3D transistors is that by wrapping around the transistor gate, a better control over electrical transport through the channel is provided. Therefore, the short channel effects (SCEs) which are an important problem for small gate lengths are reduced, resulting in a decrease of the leakage current in the transistor.

An example of SCE is drain-induced barrier lowering (DIBL). For a small gate length, the drain voltage may decrease the barrier height of the source leading to large off-state leakage. This leakage phenomenon limits practically to gate length smaller than 20 nm [5].

One way to solve this problem is to move to multigate fully depleted transistors as illustrated in Figure 1.12(a)–(e).

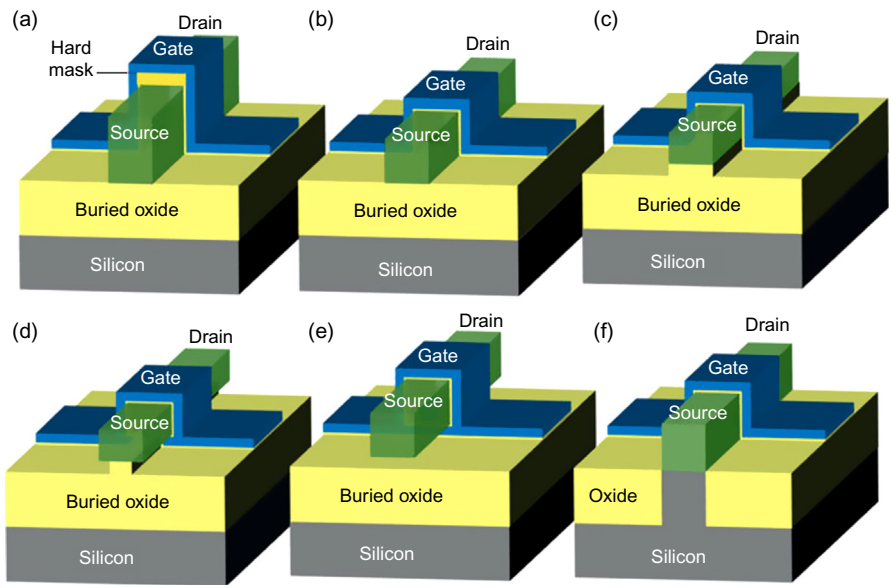

Figure 1.12a–f Schematic of 3D transistor structures: (a) SOI FinFET, (b) SOI triple-gate (or tri-gate) MOSFET, (c) SOI Π-gate MOSFET, (d) SOI Ω-gate MOSFET, (e) SOI gate-all-around MOSFET, and (f) A bulk tri-gate MOSFET. [1].

Triple-gate or tri-gate MOSFET is a 3D design for transistors which Intel introduced for 22 nm node in 2011. The most important advantage of 3D tri-gate transistors is that they operate at lower voltage decreasing significantly the active power.

Tri-gate FETs differ slightly from FinFETs. FinFET has a block material in the form of a thick dielectric on the top and is considered as a dual-gate transistor in the device terminology. The block material is introduced to avoid the forming of an inversion channel at the top part of the Si-fin (see Figure 1.12(a)). Meanwhile, the gate control in tri-gate FETs is employed on the channel region from all three sides of the device (see Figure 1.12(b)).

The gate control can be further increased compared to tri-gate by introducing a bottom side in Π-gate MOSFET (Figure 1.12(c)). In Ω-gate MOSFET, the gate control from the bottom side of the channel is improved compared to Π-gate MOSFET (Figure 1.12(d)). Both Π- and Ω-gate MOSFETs are named after the shape of their gates. If the gate is formed all around the channel, an all-around MOSFET is manufactured (Figure 1.12(e)). When a tri-gate MOSFET is formed on a bulk substrate instead of a SOI wafer, the transistor is called a bulk tri-gate MOSFET (Figure 1.12(f)).

In this group of transistors, bulk FinFET is considered as a cheaper alternative to SOI FinFET. Although the cost of the substrate is lower for bulk Si wafers compared to SOI, the fin formation needs six to eight extra process steps [6].

FinFETs may demonstrate different electrical behavior depending on how they are manufactured. For example, the dimension (width, length, and height) and shape (rectangular, trapezoidal, and triangular) of Si-fin as well as body doping level will affect the threshold voltage and carrier profile of FinFET. Sidewalls with more inclined angle and a low doping level of $\sim 10^{17}\,\mathrm{cm}^{-3}$ are required to increase the threshold voltage [7].

GATE INTEGRATION IN FinFETs

One of the issues which appears for the nanoscaled transistors is the gate formation and the integration of the high-k material and metal gate within the thermal budget of the device process (see more

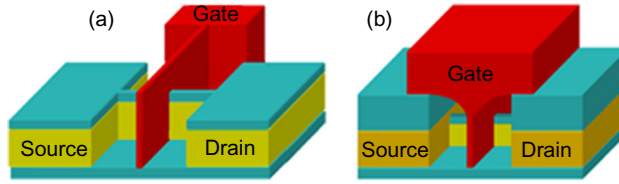

Figure 1.13 The FinFET structures with integrated (a) gate-first and (b) gate-last processes.

discussions in chapter 4). The high-k materials are amorphous and a high-temperature annealing treatment is required for their crystallization. Then either high thermally stable materials are sought or the gate should be processed last. Many research studies have compared the benefits and drawbacks of gate-first and gate-last processes for transistors (Figure 1.13).

For the gate-last process, a dummy gate is primarily processed by using SiO_2 before the selective epitaxy of SiGe in source and drain regions. Later in the process, the dummy gate is entirely removed and the high-k material is deposited in the gate region.

PARASITIC SOURCES IN MOSFET STRUCTURE

The main factors which put an end to the downscaling of planar transistors after 40 years were the parasitic capacitances and resistances. These limiting factors are eliminated significantly by transition to 3D transistors. The origin of these parasitic effects is due to the small space between neighboring devices (only few nanometers) and the shallow S/D junctions where the contact size has been truly scaled to maintain the high density in the absence of gate length scaling.

The small contact size results in higher contact resistance as well as contact-to-gate capacitance. Traditionally, the parasitic effects had no large impact on the transistor performance because they were significantly smaller than the resistance and capacitance of the channel. However, both these effects are proportional to the gate length which has been significantly reduced during the past years.

In other words, the parasitic effects became comparable or even larger than the intrinsic channel (gate and body) capacitance and resistance (see Figure 1.14(a) and (b)).

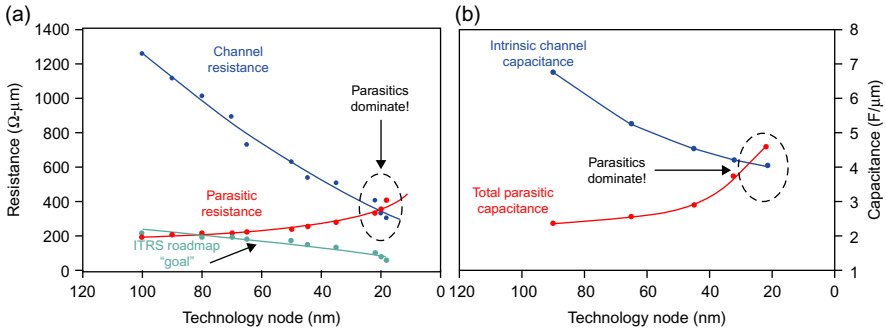

Figure 1.14 Parasitic resistances and capacitances in different technology nodes.

One of the most important parts of today's research is finding new channel materials with high carrier mobility. The parasitic resistances and capacitances are still the main obstacle for integration. As an example, carbon nanotube transistors show channel mobility of a few orders of magnitude higher than Si; however, due to the presence of parasitic resistances, the manufactured inverters are significantly slower than the state-of-the-art MOSFETS [8,9]. Another example that can be pointed out here is multigate transistors consisted of Si-fins, where the parasitic resistance to small S/D areas is higher than planar MOSFETs [10].

LITHOGRAPHY OF NANOSCALED MOSFETs

Various lithography techniques have been reviewed in Chapter 4. Here the focus is on Sidewall Transfer Lithography (STL), which is a simple and cost-effective technique to create nanoscaled transistors.

SIDEWALL TRANSFER LITHOGRAPHY

To follow the Moore's law, it is required that the number of transistors in the chip is almost doubled every 2 years. This requires a downscaling of MOSFETs both in vertical and horizontal dimensions. The gate length of MOSFETs should be thinned and therefore lithography technique to achieve the nanoscale levels becomes very critical. One concern with submicron gate lengths in planar MOSFETs or 3D FinFETs is line-edge roughness (LER) [11]. This is caused by polymer aggregates which naturally exist in photoresist films [12]. For nanoscaled MOSFETs, the LER problem results in a large line-width roughness (LWR) which degrades device performance. The STL is a method

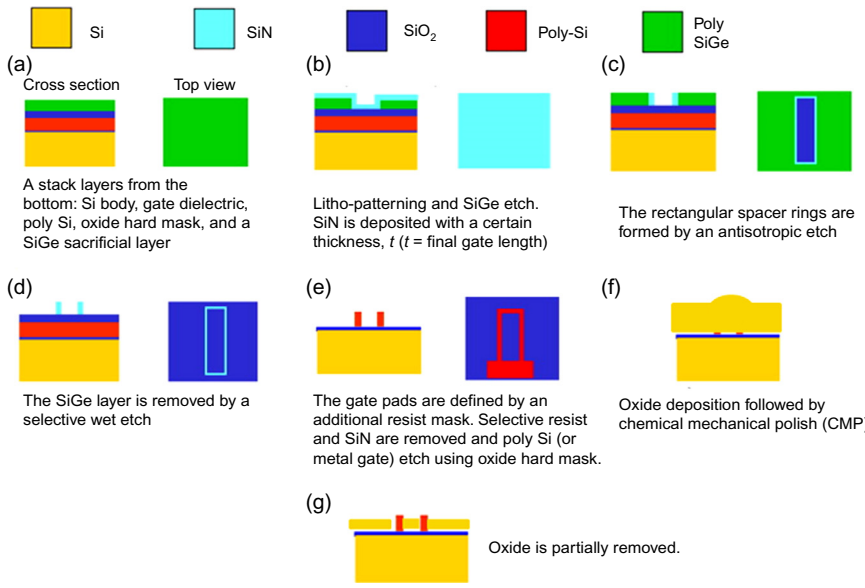
Si
SiN
SiO_2
Poly-Si
Poly SiGe
(a)
Cross section
Top view
A stack layers from the bottom: Si body, gate dielectric, poly Si, oxide hard mask, and a SiGe sacrificial layer
(b)
Litho-patterning and SiGe etch. SiN is deposited with a certain thickness, t (t = final gate length)
(c)
The rectangular spacer rings are formed by an antisotropic etch
(d)
The SiGe layer is removed by a selective wet etch
(e)
The gate pads are defined by an additional resist mask. Selective resist and SiN are removed and poly Si (or metal gate) etch using oxide hard mask.
(f)
Oxide deposition followed by chemical mechanical polish (CMP)
(g)
Oxide is partially removed.

Figure 1.15 STL process steps for FinFET fabrication.

which provides an excellent opportunity to achieve the nanoscaled dimensions without expensive lithography techniques. The STL technique is performed by a deposition and etching of sacrificial layers. Figure 1.15(a)–(g) shows the whole process to form nanowires. The main idea is deposition of a SiN layer with a thickness of the desired gate length of the transistor. The SiN is dry-etched and leaving behind SiN sidewall spacers which can be used later as hard mask for the gate formation [13].

STL technique has been successfully applied to form regular shape Si-fin with 14 nm width. A SiGe layer is deposited selectively on Si-fins using reduced pressure chemical vapor deposition (RPCVD) technique.

PART TWO: STRAIN ENGINEERING IN GROUP IV MATERIALS

Strain is a mechanical distortion caused by an exerted force to the semiconductor crystal. As a result, the electrical, mechanical, and optical properties of the semiconductor will change. The acting force is caused either by an epitaxial layer or by processing method when a

kind of stressor material is deposited on the top or on both sides of the strained layer. The direction and dimension of the exerted force is important to determine the effect of the strain. If a crystal cubic is compressed inward in x- and y-directions, then the cubic becomes elongated in z-direction and the strain is called compressive. In contrary, if the cubic is exposed to an outward force in x- and $y-$directions, then the crystal is shrunk in z-direction, and the strain is called tensile.

Group IV materials have diamond crystal structure and the strain changes the cube into a tetragonal form. Examples for compressive- and tensile-strained materials could be $Si_{1-x}Ge_x$ on Si (or $Ge_{1-x}Sn_x$ on strain-relaxed Ge) and $Si_{1-y}C_y$ on Si (or Ge on strain-relaxed $Ge_{1-x}Sn_x$), respectively. The strain in a layer resolved into vertical ($\varepsilon\perp$) and in-plane ($\varepsilon_{//}$) components are defined according to the formulas:

$$\varepsilon_{\perp} = \frac{a_{\perp} - a_b}{a_b} \quad \text{and} \quad \varepsilon_{//} = \frac{a_{//} - a_b}{a_b} \qquad \text{(1.17a and 1.17b)}$$

where the lattice constants are marked in Figure 1.16. The components of compressive strain are $\varepsilon\perp > 0$ and $\varepsilon_{//} < 0$, but for tensile strain are $\varepsilon\perp < 0$ and $\varepsilon_{//} > 0$.

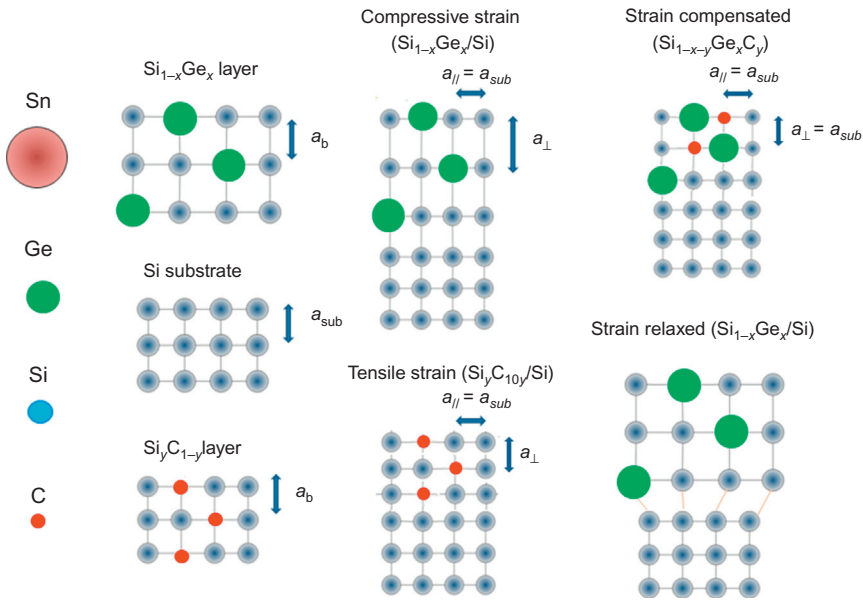

Figure 1.16 A schematic view of relaxed, strained, and strain-compensated group IV alloys.

In a similar way, mismatch parameters for crystalline layers are defined as follows:

$$f_{\perp} = \frac{a_{\perp} - a_{\mathrm{b}}}{a_{\mathrm{sub}}} \quad \text{and} \quad f_{//} = \frac{a_{//} - a_{\mathrm{b}}}{a_{\mathrm{sub}}} \qquad \text{(1.18a and 1.18b)}$$

The vertical mismatch for compressively strained crystals is $f_{\perp} > 0$ and $f_{\perp} < 0$ for tensile strain. For the strained materials, $f_{//} = 0$ when the layer is totally aligned to the substrate. The total mismatch can be obtained from $f_{\perp}$ and $f_{//}$ when the Poison ratio (ν) for the semiconductor is known [14–16].

$$f = (f_{//} - f_{\perp})\frac{1-\nu}{1+\nu} + f_{//} \qquad (1.19)$$

where ν is a value which shows how a crystal responses elastically to exerted forces and is calculated for a certain layer from the elastic constants (Table 1.1) [21]:

$$\nu = \frac{c_{12}}{c_{12} + c_{11}} \qquad (1.20)$$

It is very important to determine the elastic constants for an alloy in order to calculate the Poison ratio. For instance, the following simple approximation provides C_{ij}-values for GeSn alloy:

$$C_{ij}(\mathrm{GeSn}) = (1-x)C_{ij}(\mathrm{Ge}) + xC_{ij}(\mathrm{Sn}) \qquad (1.21)$$

In this case, a corresponding C_{ij} is determined and consequently the Poisson ratio and f-value are obtained. The Sn content in the alloy is derived with high accuracy from lattice constant for a given composition according to the following equation [22]:

$$a_{\mathrm{GeSn}}(x) = a_{\mathrm{Sn}}x + \theta_{\mathrm{SnGe}}x(1-x) + a_{\mathrm{Ge}}(1-x) \qquad (1.22)$$

where θ_{SnGe} is a constant which relates to GeSn alloying and is 0.166 Å for $x \leq 0.20$.

Table 1.1 The Elastic Constants for the Group IV Materials

Elastic Constant	Ge [17]	Sn [18]	Si [19]	C [20]
c_{11} (Mbar)	1.26	0.69	1.67	10.79
c_{12} (Mbar)	0.44	0.29	0.65	1.24

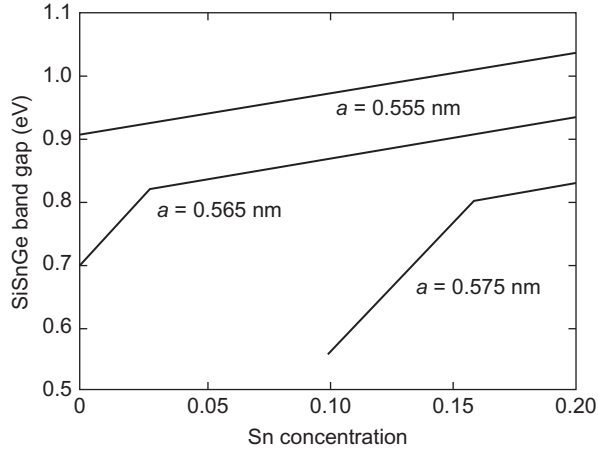

Figure 1.17 The bandgap change in ternary $Ge_{1-x-y}Si_xSn_y$ alloys with the same lattice constant [23].

The relaxation amount (R) is an important value to quantify the reduced strain upon relaxation. R is obtained according to $R = \frac{f_{\parallel}}{f}$. The R-value is expressed in percentage.

The (compressive and tensile) strain can be compensated if smaller/larger atoms are introduced in lattice to counterpart the induced compressive/tensile strain, respectively. Ternary alloys like $Si_{1-x-y}Ge_xC_y$/Si and $Ge_{1-x-y}Sn_xSi_y$/Ge demonstrate strain compensation.

The lattice constant of $Ge_{1-x-y}Si_xSn_y$ can be obtained from the following equation:

$$a_{Ge_{1-x-y}Si_xSn_y} = a_{Ge} + \Delta_{SiGe}x + \theta_{SiGe}x(1-x) + \Delta_{SnGe}y + \theta_{SnGe}y(1-y) \tag{1.23}$$

where $\Delta_{SiGe} = a_{Si} - a_{Ge}$ and $\Delta_{SnGe} = a_{Sn} - a_{Ge}$.

One of the excellent properties of the $Ge_{1-x-y}Si_xSn_y$ ternary system is the possibility to tailor separately the lattice constant and the bandgap. The bandgap may vary over a large range by tuning the Si/Sn ratio in the layers. A linear relationship between the bandgap and the Sn content is obtained for a certain lattice constant as shown in Figure 1.17. Lattice-matched $Ge_{1-x-y}Si_xSn_y$ ternary system can be grown strain-free for detection of a wide range of wavelengths [23].

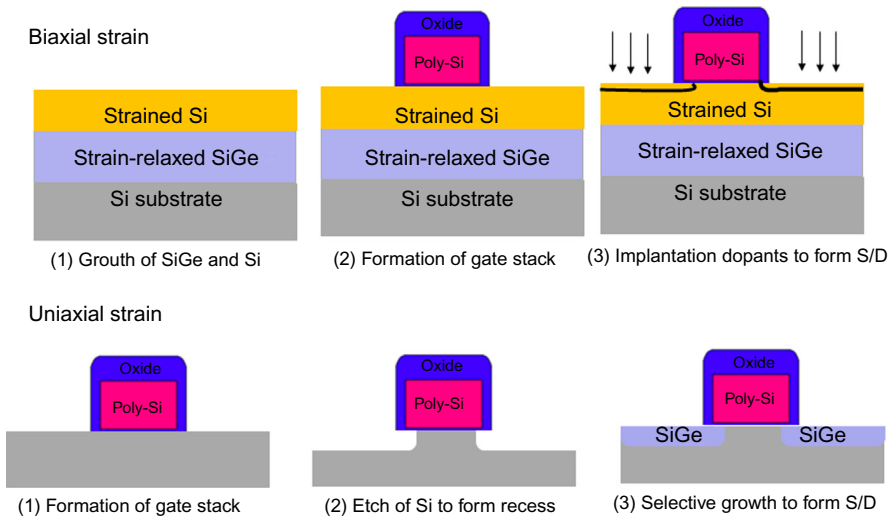

Figure 1.18 The process of formation of biaxial and uniaxial strained channel in a MOSFET structure.

STRAIN DESIGN FOR MOSFETs

There are two ways to induce strain depending on how the force is exerted: biaxial (global or 2D) and uniaxial (1D). Figure 1.18 illustrates how these types of strain are generated in silicon material.

An example for biaxial strain is when a tensile-strained Si layer is grown on strain-relaxed SiGe. A problem with such structures is that a graded SiGe layer (1 μm, 10% Ge) is used as a virtual substrate. This means that a few micrometers of SiGe are required to achieve high strain amount in the Si cap layer.

The purpose of inducing high strain amount in transistor structure is to decrease both the scattering and effective mass of carriers in the channel region.

In general, strain decreases the intraband scattering rate (where acoustic phonons are involved) by changing the density of states of LH and HH bands. The other effect of strain is to decrease the interband scattering (where optical phonons are involved) by splitting the HH and LH bands. This scattering rate is significantly reduced when the split of HH−LH bands is comparable to the energy of optical phonons. Therefore, in order to improve the carrier mobility, a stress amount larger than 1 GPa which corresponds to ∼25−30% Ge is needed [24,25].

STRAIN EFFECT ON CARRIER MOBILITY

The carrier mobility is one of the most important topics for MOSFET design. The carrier mobility is affected by the presence of defects, interfacial states (e.g., at interface of high-k materials), surface roughness, dopant concentration, channel material, and channel strain. Some basic definitions are necessary to be provided here for further advanced discussions later in the chapter.

BASIC DEFINITIONS

The carrier movement under the influence of an electric field is described by the following equation:

$$\frac{\mathrm{d}}{\mathrm{d}t}(m^* v_\mathrm{d}) + \frac{m^* v_\mathrm{d}}{\langle \tau \rangle} = qE \tag{1.24}$$

where v_d is the drift velocity, E is the electric field, m^* is the effective mass, and τ is the scattering time for the carriers. In steady state, the first term of the above equation becomes zero. Then

$$\frac{m^* v_\mathrm{d}}{\langle \tau \rangle} = qE \quad \text{or} \quad v_\mathrm{d} = \mu E$$

where the mobility is defined as $\mu = q\langle \tau \rangle / m^*$.

In order to enhance the carrier mobility, either the effective mass has to be reduced or τ to be increased. The effective mass can be changed when the curvature of the subband is changed. This can be designed by inducing strain in the crystal. Meanwhile τ is changed when the scattering of carriers during the transport in the channel is decreased. The main scattering mechanisms in the semiconductors are addressed in the following.

Defect scattering: The carriers are scattered over the lattice deformations due to the lattice potential nonuniformities. There are two categories of defects: extended defects, e.g., dislocations and stacking faults, and local defects, e.g., point defects and precipitates (or islands) in the crystal lattice. The extended defects are mostly generated as a result of strain relaxation or problems during epitaxy process. The dopants or alloying materials also induce carrier scattering and therefore are often included in the defect scattering category.

Lattice scattering: The carrier scattering due to lattice deformations or phonon vibrations in acoustic or optical forms. The acoustic phonons have energies $\hbar\omega \ll kT$, where scattering rate is low, whereas optical phonons have energies $\hbar\omega > kT$ in vibrational dispersion relationships.

Deformation potential: When the acoustic phonons vibrate the lattice atoms, the conduction and valence band edges change as well.

Piezoelectric scattering: This occurs when a local electric field forms in the lattice once its potential changes by lattice vibrations in a way that more charge accumulates in one side of the lattice. Because of the polar nature of III−V compound semiconductors, piezoelectric scattering is dominant in these materials compared to the group IV materials. In MOSFETs the carrier mobility for a drive current is derived from expression 1.15 by inserting the oxide capacitance, physical dimensions of the gate and applied voltages to the transistor terminals.

CARRIER MOBILITY IN MOSFETs WITH STRAINED Si CHANNEL

The presence of strain changes the band structure in a way that both the carrier scattering and effective mass are reduced.

The early works on strain engineering in MOSFETs were focused on biaxially strained Si channel. The driving force behind this type of transistor design was to improve the carrier mobility for both p- and n-MOSFETs at the same time [26].

To induce global strain over a wafer, a series of developments were performed by wafer manufacturers which provided strained silicon and germanium on insulator (sSOI and sGOI). Another solution for advanced strain engineering is given by SiGe on insulator (SGOI). These layers are strain-free and can be used as virtual layers for highly strained Si or SiGe layers. Dual-channel heterostructures on insulator (DHOI) is one way to process nMOSFET and pMOSFET. Figure 1.19(a)−(d) illustrates such a SGOI wafer for DHOI design where the strained Si and SiGe layers are integrated to host the hole and electron channels, respectively, in high mobility devices (as described in Table 1.2) [26].

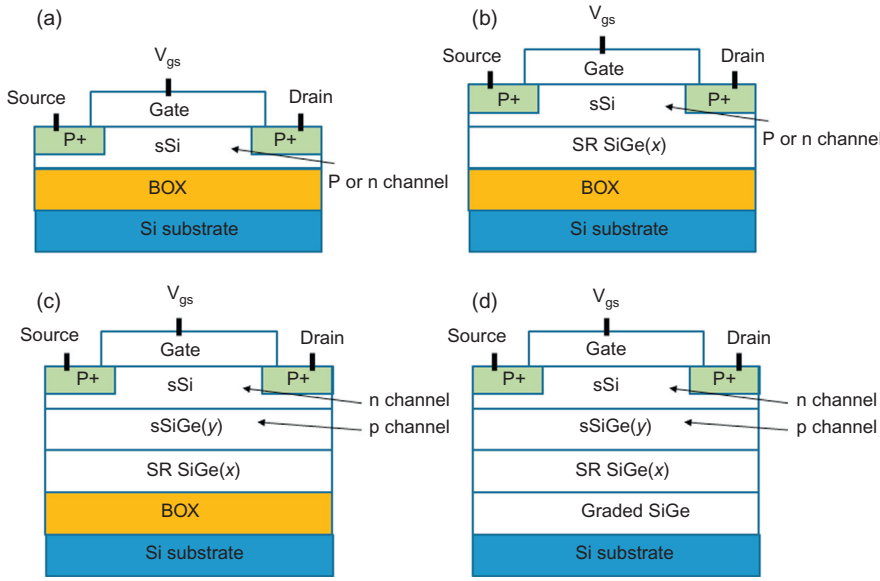

Figure 1.19 Different designs of biaxial-strained Si channel in MOSFETs [26].

Table 1.2 Descriptions of the Biaxial-Strained Si in MOSFETs	
Strained Si on insulator (sSOI) [27]	Commercially available substrates, high electron and hole mobility, no leakage between the transistors, low power consumption
SiGe on insulator (sGOI) [28]	Strain-relaxed SiGe is created through condensation technique, Si strained for high electron and hole mobility, no leakage between the transistors, low power consumption
Dual-channel heterostructure on insulator (DHOI) [29,30]	SiGe is created through condensation technique, the thicknesses can be reduced to minimize SCEs (advanced strain engineering)
Dual-channel heterostructure on bulk (DHOB) [31]	Strain-relaxed SiGe is created through epitaxy and annealing treatment high electron and hole mobility

Late in the 1990s, different analysis suggested that the industry process should be adapted to uniaxial strain. The main reasons are discussed as follows:

1. Uniaxial stress offers considerably larger hole mobility at both high and low applied electric fields because of the difference between the surface confinement for HL and HH bands (Figure 1.20).
2. Larger drive current can be obtained for uniaxial strain which is beneficial for short channel transistors. This is due to the fact that

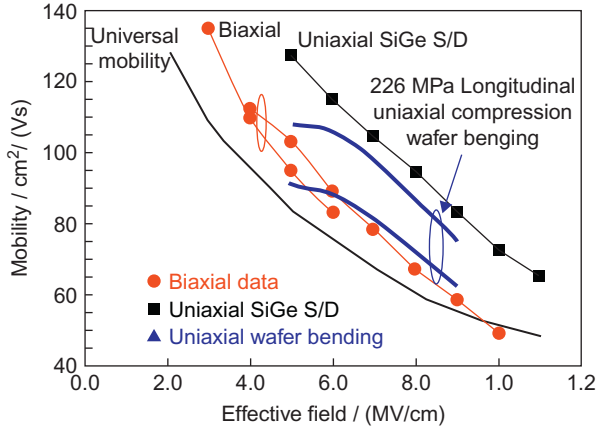

Figure 1.20 The hole mobility of pMOSFET versus vertical field for biaxial and uniaxial strained Si [32].

the enhancement in electron or hole mobility in uniaxial strain roots from reduction of the effective mass and not from decrease of scattering processes as is the case for biaxial strain.

3. The uniaxial stress provides almost five times smaller threshold voltage shift (ΔV_T) in n-channel MOSFETs. This is a very important point as this shift is usually tailored with the change of doping level in the channel region [32]. Equations (1.1a), (1.1b), and 1.2 show the relationship of threshold voltage with conduction band edge E_c, the density of states in valence band, N_V, and bandgap, E_g, as follows:

$$q\Delta V_T(\sigma) = \Delta E_c(\sigma) + (m-1)\left[\Delta E_g(\sigma) + kT\ln\frac{N_V(0)}{N_V(\sigma)}\right] \quad \text{Biaxial stress} \tag{1.25}$$

$$q\Delta V_T(\sigma) = (m-1)\left[\Delta E_g(\sigma) + kT\ln\frac{N_V(0)}{N_V(\sigma)}\right] \quad \text{Uniaxial stress} \tag{1.26}$$

According to the above equations, there are two reasons for the threshold voltage shift behavior:

1. Biaxial tensile stress results in a larger valence offset and larger bandgap narrowing in Si channel compared to uniaxial strain. As a result, LH band is maximum in biaxial stress, while HH is for uniaxial stress.
2. In uniaxial strain, the ΔE_c term makes up just a minor change since only the gate region is strained (Figure 1.21).

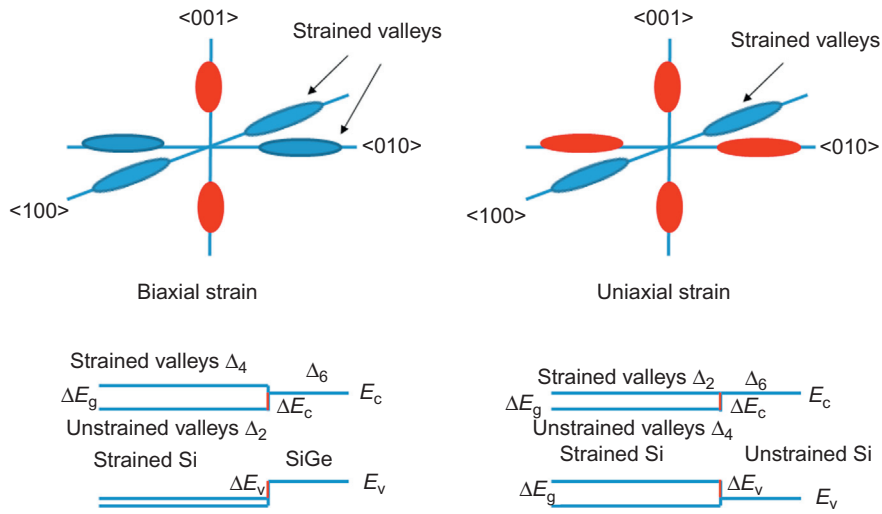

Figure 1.21 The band alignment of strained Si in biaxial and uniaxial strain [25].

In conclusion, these discussions indicate that uniaxial stress has more advantages for logic technologies compared to biaxial stress. Uniaxial strain was integrated for the first time at 90 nm node technology and will be the dominant strain type on the path of more Moore.

For industrial applications, three methods have been applied to increase the mobility: embedded or elevated SiGe-based stressors in S/D regions, SiN stress liners on the transistor and hybrid substrates. The hybrid substrate refers to wafers, e.g., with (110) orientation. High-performance ICs in many technological nodes has integrated these methods for nMOSFET and pMOSFET [33,34].

To explain the transport properties in the channel region, piezoresistance coefficients are indicators which are defined in terms of mobility's fractional variations as $\Delta\mu/\mu = \approx |\pi_{//}\sigma_{//} + \pi_{\perp}\sigma_{\perp}|$, where $\sigma\perp$ and $\sigma//$ are the transverse and longitudinal stresses, and $\pi_{//}$ and $\pi_{\perp}$ stand for the piezoresistance coefficients in longitudinal and transverse directions. The piezoresistance coefficients can be expressed in terms of fundamental cubic piezoresistance coefficients $\pi 11$, $\pi 12$, and $\pi 44$ or their combinations for a certain orientation [35].

The piezoresistance coefficient for holes is highest for compressive strain along ⟨110⟩ for both (001) and (110) wafers. Therefore, ⟨110⟩

channel direction has been widely used in industrial applications utilizing strained Si technologies [33,36].

STRAIN AND CRITICAL THICKNESS

Global Critical Thickness of SiGe Layers

All types of strained alloys store mechanical energy which may relax after their thickness exceeds a critical value. In the case of a large misfit, this critical thickness is very thin and the material may relax after only a few monolayers.

Historically, the first mathematical model to predict the critical thickness was presented by Matthews−Blakeslee (MB) in the 1970s. The model, known as equilibrium model, presents a balance between two forces during epitaxy: F_T which favors to form misfit dislocation and F_a to relief this force during epitaxy. If $F_a < F_T$, the strained material is deposited without any formation of dislocations. A critical thickness is calculated when $F_T = F_a$. The critical thickness is given by [37]:

$$h_c = \frac{1 - \nu \cos^2 \theta}{1 + \nu} \frac{b}{8\pi f \cos \lambda} \ln \frac{\alpha h_c}{b} \tag{1.27}$$

A few years later when the epitaxial technique for SiGe layers was developed, a large discrepancy between the theoretical calculations and experimental data was observed. One way to explain this large discrepancy is that the MB theory takes into account only a balance between two acting forces to form misfit dislocations and it lacks consideration of the interaction, nucleation, and propagation of misfit dislocations. Therefore, the critical thickness for SiGe layers was remarkably underestimated.

The experimental values were later modeled and fitted by People and Bean [38]:

$$h_c = \frac{1 - \nu}{1 + \nu} \frac{\sqrt{2}}{32\pi} \frac{b^2}{af^2} \ln \frac{h_c}{b} \tag{1.28}$$

A more sophisticated model was introduced by Dodson and Tsao (DT) when the concept of equilibrium forces was replaced by excess stress σ_{ex} between the mentioned forces in MB [39,40]. Therefore, the

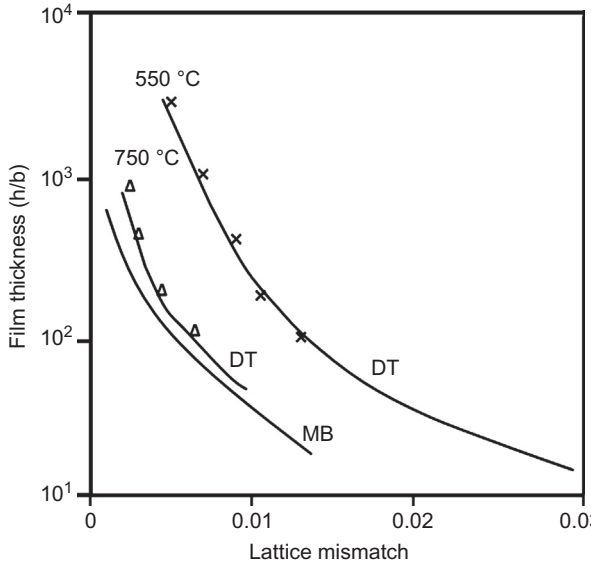

Figure 1.22 The calculated critical thickness of SiGe layers versus Ge content from DT model [39,40], where MB is from the equilibrium model [37]. The (×) and (Δ) marks are experimental data for the grown SiGe layers [38].

strain relaxation may occur if the nonzero σ_{ex} is set to zero. The MB equation is then retrieved again. σ_{ex} is expressed by

$$\frac{\sigma_{ex}}{\mu} = 2\varepsilon\frac{1-\nu}{1+\nu} - \frac{b}{2\pi h}\frac{1-\nu\cos^2\theta}{1-\nu}\ln\frac{4h}{b} \tag{1.29}$$

where μ is the shear modulus and ε is the elastic strain. Figure 1.22 illustrates the experimental data reported from different groups and the calculated thickness for SiGe layers from DT and MB theories (when a critical $\sigma_{ex}/\mu = 0.026$ is reached). The region indicated between MB and DT thickness is called metastable. Most of the strained layers are grown with a thickness which places them in the metastable zone. A good consistency between the layer thickness and Ge content is observed. The metastable region for SiGe is a result of both equilibrium and nonequilibrium theories which considers the generated stress. In general, the stress in the epi-layers is temperature dependent. This means that the metastable region may become smaller or larger for high and low growth temperatures.

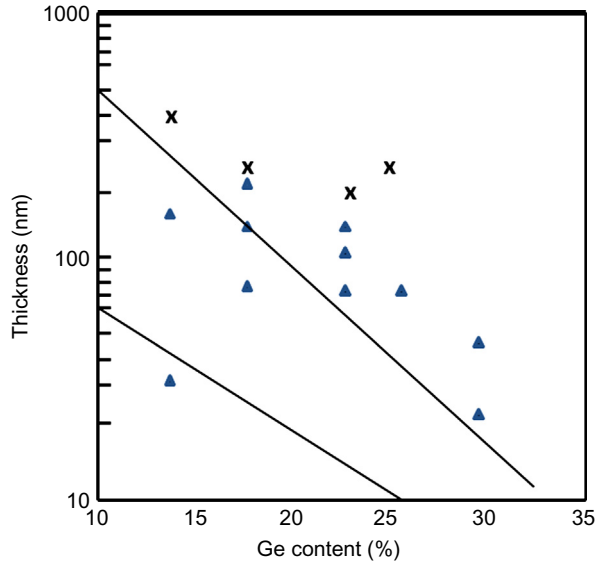

Figure 1.23 The experimental data showing thickness of strained (▲) and partially strain-relaxed (×) SiGe versus Ge content [41].

CRITICAL THICKNESS OF SiGe LAYERS ON PATTERNED SUBSTRATES

The above experimental data and theories are for the SiGe layers grown on the whole wafer. The kinetics of the growth is quite different if the SiGe layers are grown selectively on the patterned substrates [41].

On a patterned substrate comprising openings in the oxide layer grown on top of a Si wafer, SiGe is strained in the center of oxide openings and is (partially) relaxed in the areas close to the oxide walls. This kind of strain distribution creates a media where the misfit dislocations may get depleted in the relaxed area. The presence of relaxed areas will also change entirely the kinetics of misfit dislocations and their propagation. This provides the possibility to grow strained SiGe layers selectively far above the critical thickness as shown in Figure 1.23. The presence and kinetics of defect propagation is affected in the presence of strain.

CRITICAL THICKNESS OF SiGe LAYERS GROWN ON NANO FEATURES

The recent reports have demonstrated that the strain relaxation of SiGe is delayed once grown on nanoscaled areas [42]. In FinFET

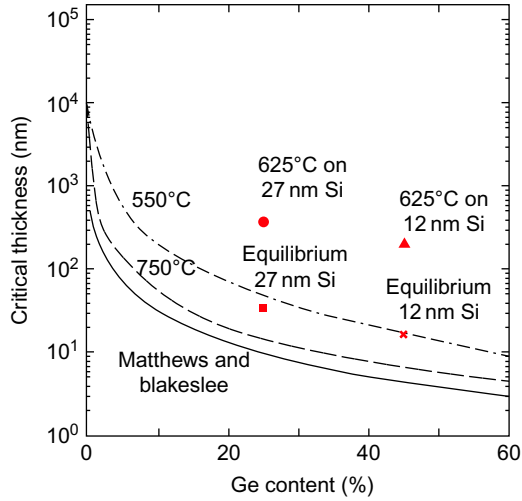

Figure 1.24 The critical thickness of SiGe layers grown on Si fins with different sizes [42].

structure, SiGe is grown on the Si-fin to raise the S/D areas. In this case, high-quality SiGe with a thickness far beyond the reported critical thickness for bulk material is observed. A reason for this behavior is that the strain forces on the fin are dependent both on the thickness of the Si fin (substrate) and the thickness of the grown layer. Since the strain relaxation of SiGe layers occurs through the formation of 60° dislocations which glide on {111} planes, the shape of the Si fin has an important role in the strain relaxation process. Therefore, the maximum-induced strain changes in terms of the fin/film thickness as well and is not directly related to the film thickness. As a result, the critical thickness of SiGe layers grown on Si fin is significantly increased compared to the bulk form as shown in Figure 1.24.

STRAIN MEASUREMENTS AND APPLICATIONS

Strain Measurement

There are three powerful techniques to measure strain in semiconductors: Raman spectroscopy, transmission electron microscopy (TEM), and high-resolution X-ray diffraction (HRXRD).

Raman Spectroscopy

This technique is a nondestructive method to measure strain in semiconductors. The technique is based on inelastic scattering of light

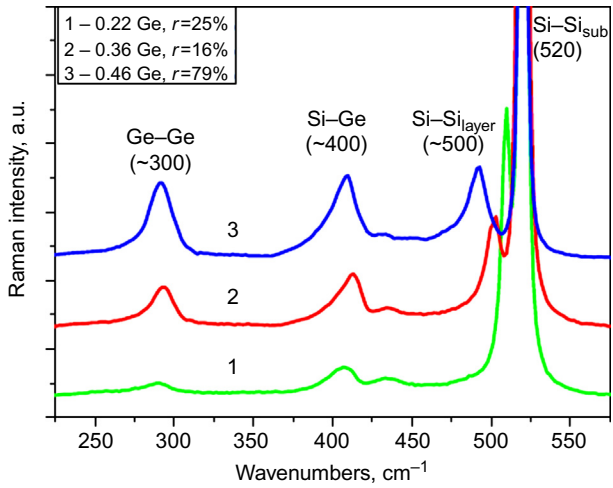

Figure 1.25 Raman spectra for strained SiGe/Si samples with different Ge contents.

(wave number in cm^{-1}) as a result of lattice vibrations and electronic excitations. The frequency shift of scattered light can be determined by comparing the signal from unstrained and strained layers. The frequency shift is interpreted to strain amount in the layer.

For a SiGe/Si structure, the three peak positions, Si—Si, Si—Ge, and Ge—Ge phonon modes, will be of interest as shown in Figure 1.25 [43].

This analysis offers a micro-Raman mapping which can measure the strain variations over an area with 1 μm resolution. The technique can be combined with AFM in order to obtain an accurate position on the sample [44].

In a Raman spectra, the relative energies and intensities of the Si—Si, Si—Ge, and Ge—Ge vibrations are dependent on the relative number and distortion of corresponding bonds in the alloy due to composition and strain, respectively [45,46]. This dependency of phonon frequency in terms of strain amount in SiGe layers, ε, is given by

$$\omega_{SiSi} = 520.2 - 62x - 815\varepsilon \tag{1.30}$$

$$\omega_{SiGe} = 400.5 + 14.2x - 575\varepsilon \tag{1.31}$$

$$\omega_{GeGe} = 282.5 + 16x - 385\varepsilon \tag{1.32}$$

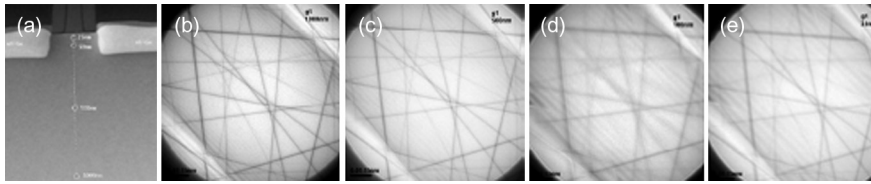

Figure 1.26 (a) Dark field image of a test structure with SiGe in S/D and CBED patterns at different distances from the top, (b) 1000 nm, (c) 500 nm, (d) 100 nm, and (e) 25 nm.

The third term (containing ε) is associated to strain where the first and second terms relate to relaxed SiGe material [44–47].

TEM Analysis

The convergent beam electron diffraction (CBED) in TEM is a technique to measure the local strain in nanoscale resolution. The technique has been applied to measure the strain in MOSFET's channel region. The main point is using high-order Laue zone (HOLZ) deficient lines which are sensitive to variations of lattice parameter. The strain is estimated when the Holtz patterns are simulated and compared to experimental results. Figure 1.26(a)–(e) illustrates how the HOLZ lines are changed when the strain is decreased on the path away from the channel. The accuracy of CBED technique is 2×10^{-4}.

A concern about applying CBED pattern method is the strain relaxation when e-beam is emitted to an area. The strain relaxation appears in the form of split of HOLZ lines and has to be taken into account in the simulations.

The other major problem with using CBED patterns is that the sample area has to be at least 200 nm thick in order to obtain a sharp pattern. This means that it is difficult to apply CBED for analysis of MOSFETs with ultrathin channel length. Therefore, in many cases, a test structure is analyzed and the results are correlated afterward to smaller dimensions [48].

High-Resolution X-Ray Analysis

Among the characterization techniques, XRD is the most popular one since it is a fast and a nondestructive method. X-ray rocking curves (RCs) are one-dimensional (1D) scans around a certain

reflection in the reciprocal space. RCs are also known as $\omega - 2\theta$ scans, where ω and 2θ are incident and diffracted beams, respectively. The analysis is based on the Bragg law, $2d \sin\theta = n\lambda$, where d is the inter-planar distance, θ is the incident X-ray beam, and λ is the wavelength of $K_{\alpha 1}$ of copper which is 0.15406 nm. The strained layers experience a distortion in lattice constant in the z-direction, where d is either elongated or shrunk depending on the type of strain. When a multilayer structure contains layers with different strain amounts and types, θ shifts according to d-values and different peaks are generated during scanning. The position of layer peaks relative to the substrate peak reveals the nature and amount of strain of epi-layers. A series of fringe peaks may also appear in RCs which are generated from the interference of X-ray beam within the strained layers. The material composition is measured from layer and substrate peak positions and the layer thickness from two neighboring fringes in the RC.

The defect density can be estimated by measuring the full-width-half-maxium (FWHM) of peaks in the RC.

The misfit parameters ($f_{\perp}$ and $f_{//}$) can be measured by high-resolution reciprocal space mappings (HRRLMs) which are 2D measurements around a certain reflection in reciprocal space [14–16]. Four input parameters (ω and 2θ for layer and substrate) are obtained from an HRRLM and misfit parameters can be calculated. HRRLMs in (113) reflection direction are the most sensitive ones for measurement of strain relaxation and defects. This is due to the low grazing angle of X-ray beam (ω is 2.8°) which covers a large area of sample during the measurement.

HRRLMs and RC scans can be performed to measure strain in SiGe over chips on patterned substrates when the X-ray beam could be focused on a large array of the MOSFETs. Recently, (113) HRRLMs have been applied to measure strain over chips with 22 nm transistor nodes as shown in Figure 1.27(a) and (b) [48]. The figure shows the HRRLMs of intrinsic and B-doped SiGe layers grown in recess S/D of transistors. The B concentration can be estimated by comparing the intrinsic and doped SiGe layers' RCs and measuring the layer shift. This shift is originated from the strain compensation of B in SiGe matrix and is interpreted to the dopant concentration.

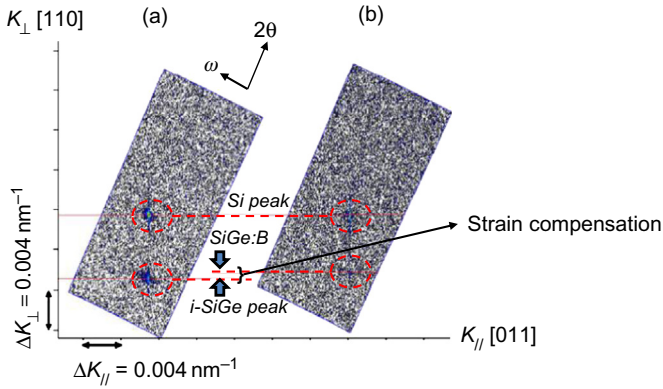

Figure 1.27 HRRLMS around (113) reflection of an array of 22 nm transistors containing $Si_{0.65}Ge_{0.35}$ layers in S/D region: (a) intrinsic layer and (b) B-doped with concentration of 3×10^{20} cm^{-3}. The shift of SiGe:B peak (toward Si peak) compared to i-SiGe is due to the strain compensation [49].

The drawback with X-ray technique is the impossibility of locally distinguishing the strain in the transistor structures; the technique can only provide information over a large array of devices.

PART THREE: CHEMICAL VAPOR DEPOSITION OF GROUP IV MATERIALS

CVD refers to a process in which certain precursor gases decompose over a substrate inside a reactant chamber at a specific growth temperature. There are several precursors for Si epitaxy depending on the growth temperature and application: silane (SiH_4), dichlorosilane (SiH_2Cl_2), trichlorosilane ($SiHCl_3$), tetrachlorosilane ($SiCl_4$), disilane (Si_2H_6), and trisilane (Si_3H_8). For Ge epitaxy, germane (GeH_4) and digermane (Ge_2H_6) are the common sources. There are also a variety of $(H_3Ge)_xSiH_{4-x}$ ($x = 1-4$) compounds for the growth of Ge-rich SiGe layers [50]. The dopant precursors are diborane (B_2H_6) for p-type doping and phosphine (PH_3) and arsine (AsH_3) for n-type doping. ($As(GeH_3)_3$ is a gas source which is also used for n-type doping of SiGe layers at low growth temperature [50]. These sources are usually diluted in hydrogen. For Sn, SnD_4 and $SnCl_4$ are the most practical and common sources. Methylsilane (SiH_3CH_3) is widely used for carbon doping in Si and SiGe layers.

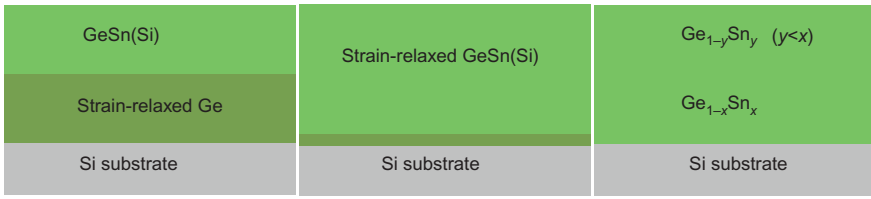

Figure 1.28 Schematic of structures where GeSn can be grown strained or strain-relaxed.

Ge—Sn—Si alloys are known for at least two decades for their potential for indirect-to direct bandgap transition [51]. At first, these alloys were epitaxially deposited by molecular beam epitaxy (MBE) [52]. However, the growth of these alloys using CVD technique was not demonstrated until recently when a stable Sn precursor, like SnD_4, was produced [53,54]. Although this precursor has demonstrated impressive results, the SnD_4 molecule has a limited lifetime and dissociates into Sn and deuterium after a while. The stability problem can be partly solved when SnD_4 is diluted in hydrogen prolonging the lifetime to a few months.

Another source for Sn is $SnCl_4$ which is widely used to grow Sn oxides by atomic layer deposition (ALD). This source is in liquid form, is converted into gas form, and later a stable gas flux of $SnCl_4$ molecules is introduced into the CVD reactor. GeSnSi layers with high Sn content and high layer quality have been deposited in temperature range of 290—380°C [53,54]. Figure 1.28 illustrates how to grow GeSn layers with different strain types.

SELECTIVE AND NONSELECTIVE EPITAXY

If a layer is deposited on the entire wafer, the epitaxy is called nonselective. Otherwise, a selective epitaxial growth (SEG) on patterned substrates can be performed where the growth takes place only on exposed Si areas inside oxide (or nitride) openings. This type of epitaxy occurs when HCl is introduced during deposition. The dissociated Cl atoms act as Si etchant and remove nucleated Si on the oxide (or nitride).

The SEG found a key application in MOSFETs and photonic components [55]. SiGe can be deposited selectively as stressor material in S/D regions to create uniaxial compressive strain in the transistor channel and enhance the hole mobility in pMOSFETs [32].

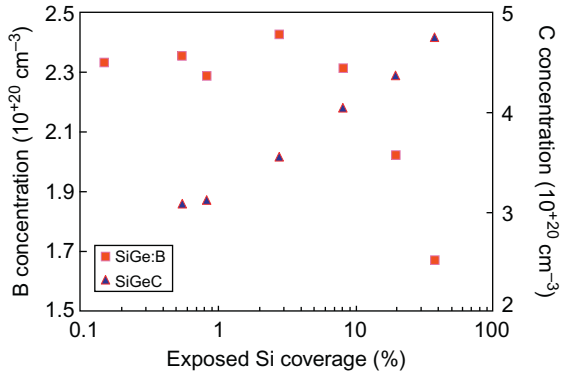

Figure 1.29 The variation of B and C concentration in SiGe layers grown selectively on chips with different coverage of exposed Si areas. Dichlorosilane, germane, methylsilane, HCl, and diborane partial pressures were 60, 1.2, 0.3, 20, and 3.6 mtorr, respectively [56].

Although selective epitaxy is a very attractive deposition technique for MOSFETs, this growth method suffers from facet formation, nonuniformity of layer profile inside the oxide openings (micro-loading), or over different parts of a chip or wafer (global loading or pattern dependency) [56–59].

The nonuniform deposition is also observed from wafer to wafer when the thickness of oxide or nitride on the wafers is changed. This growth problem leads to uncontrolled Ge content and growth rate (layer thickness) over the chip area. As a result, the incorporation of boron (or carbon) in SiGe is affected and the sheet resistance in S/D junctions will not be uniform as well (Figure 1.29).

Many investigations have been carried out to find methods to improve the uniformity of growth and to decrease the pattern dependency to $<5\%$ [57,58], but so far there is no remedy to totally eliminate this problem.

The reason for pattern dependency links to the gas kinetics and nonlinear consumption of the gas molecules over a patterned wafer [56,59]. The kinetics of CVD growth can be described by the established boundary stream theory assuming a laminar gas flow over the Si wafer as illustrated in schematic view in Figure 1.30 [59]. For the growth of SiGe layers in S/D regions in planar MOSFETs, the layout of the chip (size, shape, and density of openings) is an essential matter.

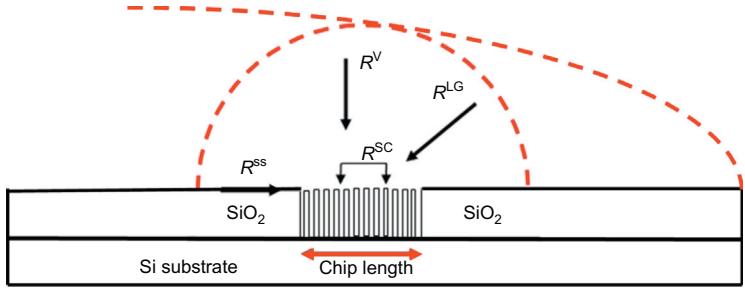

Figure 1.30 Schematic view of the gas boundary when laminar gas stream flows over the patterned substrate during the CVD process. The black arrows show the movement of gas molecules toward a chip [59].

The gas molecules move within streams and diffuse down through the boundaries. These diffused gas molecules are attracted toward the exposed Si areas and are consumed by dangling bonds. In the case of patterned substrates containing chips with opening arrays, a gas depletion volume is established as shown in Figure 1.30.

The total growth rate (R_{tot}) considering all the contributing components is expressed as

$$R_{Tot} = R_{Si}^{V} + R_{Si}^{LG} + R_{Si}^{SS} + R_{Si}^{SC} + R_{Ge}^{V} + R_{Ge}^{LG} + R_{Ge}^{SS} + R_{Ge}^{SC} - R_{E}^{V} - R_{E}^{LG} - R_{E}^{SS} - R_{E}^{SC} \quad (1.33)$$

where R_V and R_{LG} represent the reactant gas molecules in vertical and lateral directions, while R_{SS} and R_{SC} denote the dissociated molecules on the oxide (or nitride) surface around or within a chip. The R_E terms stand for the etch rate caused by the HCl etchant species.

In order to reduce the pattern dependency of the growth, the lateral components in Eq. (1.33) have to be decreased.

Various methods have been suggested to reduce the pattern dependency of SiGe layers.

High HCl partial pressure decreases fast the density of species on the oxide surface, and the contribution of R_{SS} and R_{SC} components will be eliminated.

Another growth parameter which may affect the lateral components is the carrier gas velocity controlled by the total pressure in the reactor.

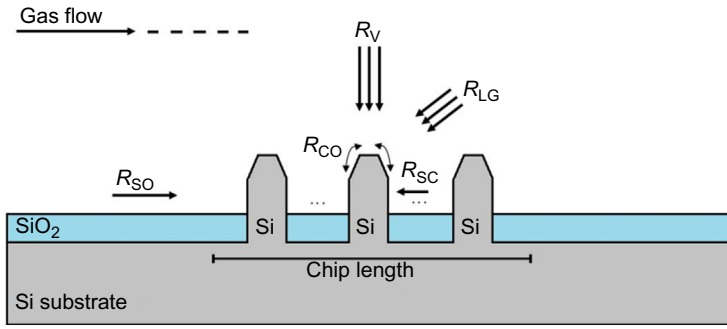

Figure 1.31 Schematic view of the gas boundary during the CVD process when the laminar gas stream flows over a patterned substrate containing Si-fin. The black arrows show the movement of gas molecules toward a chip [60].

When the thickness of gas depletion volume is decreased, a faster diffusion of the gas molecules to the surface is occurred. High partial pressure of H_2 carrier gas will also give a similar effect. Therefore, a combination of low growth pressure (10 torr) and high H_2 carrier gas (40 slm) will solve the pattern dependency behavior [59].

For the 3D growth of SiGe over Si-fins or Si wires (for 14 nm technology node and beyond) Eq. 1.33 is modified by adding a component for diffusive molecules over Si surface (R_{CO}) (Figure 1.31). The Si fins can be processed for different shapes, e.g. rectangular, trapezoid. In this case, such fins may contain a series of facet planes (for a trapezoidal fin has (100) and (111) planes) and during epitaxy new facet planes are formed at the sides and bottom side of the fin as well.

The total growth rate for 3D growth is written as [60]

$$\begin{aligned} R_{\text{Total}} = {} & R_{\text{Si}}^{\text{V}} + R_{\text{Si}}^{\text{LG}} + R_{\text{Si}}^{\text{SO}} + R_{\text{Si}}^{\text{CO}} + R_{\text{Si}}^{\text{SS}} + R_{\text{Ge}}^{\text{V}} + R_{\text{Ge}}^{\text{LG}} + R_{\text{Ge}}^{\text{SO}} \\ & + R_{\text{Ge}}^{\text{CO}} + R_{\text{Ge}}^{\text{SS}} - R_{\text{HCl}}^{\text{V}} - R_{\text{HCl}}^{\text{LG}} - R_{\text{HCl}}^{\text{SO}} - R_{\text{HCl}}^{\text{CO}} + R_{\text{HCl}}^{\text{SS}} \end{aligned} \tag{1.34}$$

According to the diffusion theory, the atoms on inclined planes have a longer diffusion length compared to (001) plane. Therefore, in 3D growth a flow of atoms from inclined planes at the sides is formed towards the (001) plane in central part of Si-fins [60].

However, a diffusion length of hundreds nanometers is estimated for Si and Ge atoms for growth at 600−700 °C, which is significantly

larger than the width of a Si fin. This means the atoms may diffuse over the entire Si fin. Since the diffusion length of atoms is very large no interaction between the facet planes on the top and bottom of fin is expected. In this case R^{CO} term can be neglected in eq. (1.34).

However, if the dimensions (x, y and z) of the fin was enough large then the kinetics over the contribution of R^{CO} term in eq. 1.34 should be taken into account [60]. Calculating all the components in Eqs. (1.33) and (1.34) needs a tedious work. An empirical model has been applied to calculate the total growth rate in Eqs. (1.33) and (1.34) as following:

Free dangling bonds — Effect of SiH_2Cl_2 — Effect of GeH_4 — Effect of HCl

$$R_{Total} = \beta \frac{\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{SiH_2Cl_2}}{\left(2\pi m_{SiH_2Cl_2} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{SiH_2Cl_2 on\ Si}}{k_b T}+1\right) \exp\left(-\frac{E_{SiH_2Cl_2\ on\ Si}}{k_b T}\right)$$
$$+\chi \frac{(1+m_r)\left(1-\theta_{H(Si)}-\theta_{Cl(Si)}\right)}{N_0} \frac{P_{GeH_4}}{\left(2\pi m_{GeH_4} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{GeH_4 on\ Si}}{k_b T}+1\right) \exp\left(-\frac{E_{GeH_4 on\ Si}}{k_b T}\right)$$
$$+\chi \frac{(1+m_r)(1-\theta_{H(Si)}-\theta_{Cl(Si)})}{N_0} \frac{(BP_{GeH_4} \ln(1/c))}{\left(2\pi m_{GeH_4} k_b T\right)^{\frac{1}{2}}} \left(\frac{E_{GeH_4 on\ Si}+0.1\ eV}{k_b T}+1\right) \exp\left(-\frac{E_{GeH_4 on\ Si}+0.1\ eV}{k_b T}\right)$$
$$-\frac{\gamma}{N_0} \frac{P_{HCl}^{0.596}}{\left(2\pi m_{HCl} k_b T\right)^{\frac{\alpha}{2}}} \left(\frac{E_{Etching}}{k_b T}+1\right) \exp\left(-\frac{E_{Etching}}{k_b T}\right) \tag{1.35}$$

where E and P stand for activation energy and partial pressure of the reactant gases, and θ parameters denote the occupied dangling bonds in presence of H and Cl on Si with a specific surface orientation and temperature. The constants β, χ, and γ are tooling factors which are dependent on gas kinetics and the temperature distribution in the CVD reactor. In Eq. (1.35), the term c relates to the pattern layout of the chip which is the main factor for the pattern dependency behavior of the growth.

During selective epitaxy, the Cl atoms remove the nucleated islands on the oxide (nitride surface). In this etch process, Cl reacts mostly with Si. As a result, Ge atoms are the most probable atoms on the oxide surface. To have this considered, an additional energy term of 0.1 eV has been added to germane activation energy to consider the diffusion of Ge on oxide surface. In Eq. (1.35), m_r is Ge reaction factor on Si surface and is estimated to be 2. This factor takes into account the influence of Ge atoms to enhance the number of the dangling bonds. Eq. (1.35) can be used for both 2D (to fill out the recess or elevate source/drain) and 3D (Si fins) growth. The difference between 2D

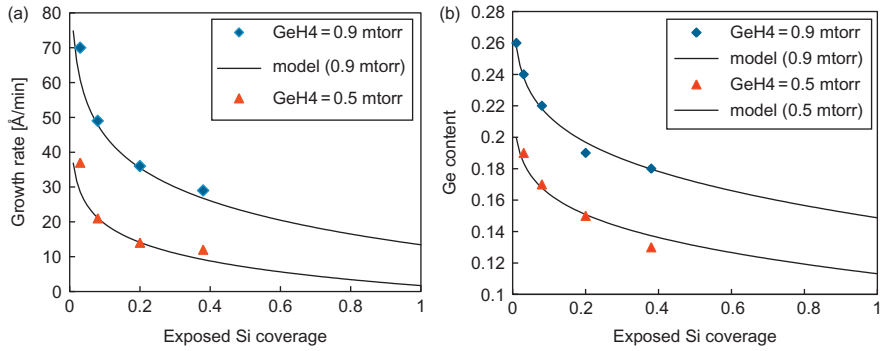

Figure 1.32 (a) Growth rate and (b) Ge content versus chip exposed Si coverage for different globally patterned wafers. The applied total pressure was 20 torr and partial pressures of HCl and germane were 60 and 20 mtorr, respectively [61].

and 3D growth is the input parameters. In 3D growth, the Si fin contains facet planes where the available dangling bonds has be to modified.

The Ge content (x term) in SiGe layers is acquired from a ratio of Si and Ge partial pressures. This is expressed as follows:

$$\frac{x^2}{1-x} = \alpha \exp\left(\frac{0.7\ \text{eV}}{k_b T}\right)\left(\frac{P_{GeH_4} + (BP_{GeH_4} \ln(1/c)) - (1-\lambda)P_{HCl}}{P_{SiH_2Cl_2} - \lambda P_{HCl}}\right) \tag{1.36}$$

where λ is a reaction ratio which represents the fraction of Cl atoms which interact with Si and Ge atoms. The value of this ratio is close to 1 for $P_{HCl} < PS_{iH2Cl2}$ and is 0.8 for high HCl partial pressures.

Equations (1.35) and (1.36) have been applied to calculate the SiGe profile grown on chips with different layouts. Figure 1.32(a) and 1.32 (b) shows a good consistency of the calculated and the experimental data.

All these calculations are for chips with uniform layout (according to Figure 1.32(a) and 1.32(b)), but this is an ideal case and for advanced chips, the layout is not uniform. A series of investigations have applied an interaction theory between neighboring chips on a Si wafer. The main equation comes from an empirical model which shows the variation of growth rate. This equation has an exponential behavior in terms of the distance, d, from a chip where the whole

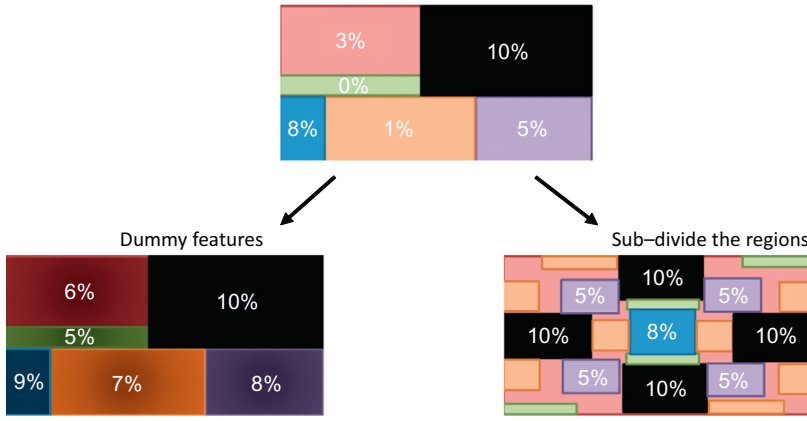

Figure 1.33 Modification of pattern distribution to obtain a uniform SiGe deposition [61].

interaction range is estimated to be τ. In this situation, the gas consumption becomes nonuniform over a chip or from chip to chip. On a patterned substrate, the dominant chips (R_{trap}) are the ones with more exposed Si area compared to surrounding chips (R_{Surr}). The growth rate of a chip under influence of a trap chip is $R_{\text{T}}(d)$ [61]:

$$R_{\text{T}}(d) = R_{\text{Trap}} + (R_{\text{Surr}} - R_{\text{Trap}})\left(1 - e^{\frac{-d}{\tau(c_{\text{surr}})}}\right) \tag{1.37}$$

The interaction length is dependent on the coverage of the chip since they are the dangling bonds which attract the gas molecules toward themselves. In order to have a uniform growth over a chip, uniform gas consumption is required. Figure 1.33 illustrates a nonuniform chip and the way to change the layout to achieve uniform deposition. Six regions are distinguished in the figure with exposed Si coverage areas of 0%, 1%, 3%, 8%, and 10%. The interaction between these regions has to be calculated mutually. The main trap regions are 8 and 10 in this chip. Uniform gas consumption over this chip is obtained either by introducing dummy features or by subdividing the trap regions over the chip. Another way to achieve the goal is to apply both methods.

PART FOUR: IMPROVEMENT OF THE CHANNEL MOBILITY

EFFECT OF RECESS SHAPE IN S/D

In MOSFETs, the channel mobility is directly linked to the strain amount in the channel region. Many investigations have paid attention on how

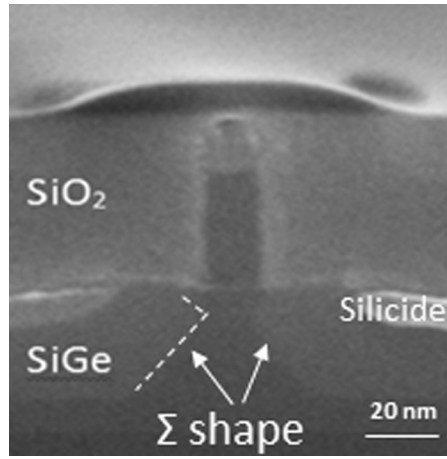

Figure 1.34 Sigma (Σ) shape recess in S/D of 22 nm bulk SiGe MOSFETs [49].

stress is exerted by SiGe in S/D region to the channel region. One way to increase the stress is to increase the Ge content. The Ge content has continuously been increased from 18% to 40% from 90 to 32 nm technology node. However, there is no more possibility for further increasing the Ge content since the defect density increases significantly due to strain relaxation in SiGe layers. The other way is to engineer the shape of the recess in S/D region. The idea behind is that the critical thickness and defect density depend on the surface facets in the recess bottom shape. This is explained by the difference of nucleation rate of SiGe layers on different facet planes. As an example, the SiGe layers deposited on the (110) facet plane show more roughness and have higher defect density compared to the (001) surface due to higher nucleation on (110) than (001).

The traditional U or square shape recess which has been used in some technological nodes consists of (110) surface and therefore is not optimized for highly strained SiGe layers [62].

In the later years, the recess shape was optimized to a sigma (Σ) shape S/D. This shape consists of (111) and (001) surfaces and was shown the most proper shape for pMOSFET application [48] (Figure 1.34).

The sigma shape increases the channel stress since the force to surface channel is from the sidewall toward the top surface. Figure 1.35 shows the effect of different recess shapes on the stress amount and carrier mobility [63].

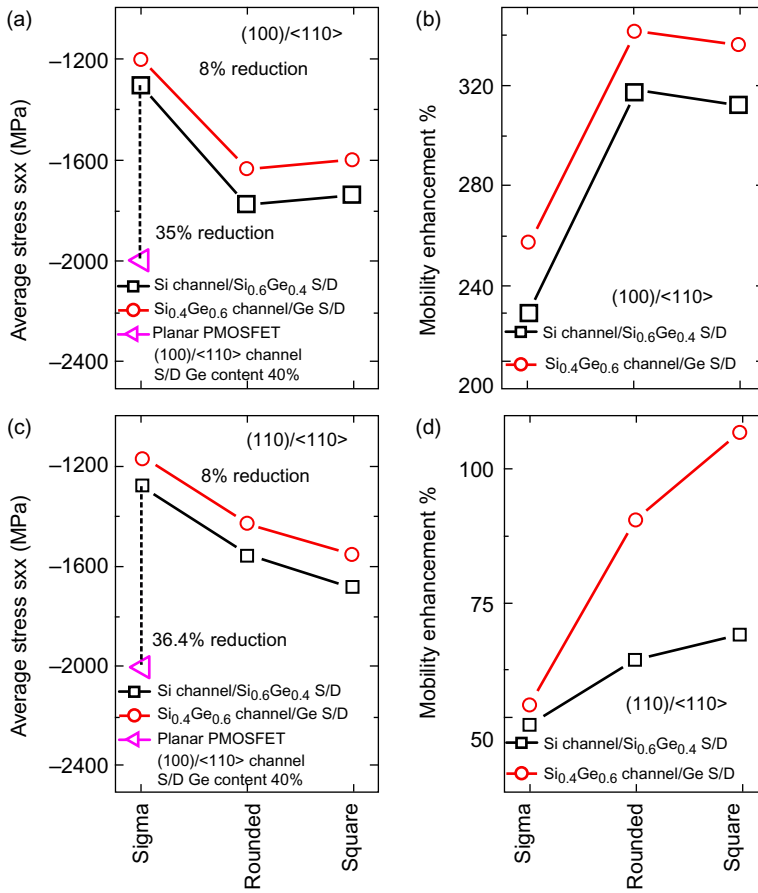

Figure 1.35 The stress and the corresponding mobility enhancement for different recess shapes for S/D region [63].

CHANNEL MATERIALS AND MOBILITY

III–V Materials

The carrier mobility in channel is an important characteristic of MOSFETs. As discussed in Chapter 1, strain can be induced in different ways in the channel region and improve the carrier transport, but it seems that the mobility enhancement cannot be continued for beyond 14 nm node. Thus, search for new channel material is ongoing to replace Si. Graphene and graphene-like materials with excellent mobility data could be good candidates for future transistors but at the moment being, they lack a reliable manufacturing method over the whole Si wafer.

Table 1.3 Material Data for Well-Known III–V Materials and Compares Them with Si and Ge

Material	Si	Ge	GaAs	InP	InAs	InSb
Lattice constant (Å)	5.431	5.658	5.653	5.869	6.058	6.749
Bandgap (eV)	1.12	0.66	1.42	1.34	0.35	0.17
Hole mobility (cm^2/V-s)	450	1900	400	200	500	850
Electron mobility (cm^2/V-s)	1400	3900	8500	5400	40.000	77000

Some studies propose III–V materials (GaAs, InP, InAs, and InSb) as channel material [64]. The main idea behind is to use the low electron mass of III–V semiconductor due to their small bandgap (Table 1.3). The low electron mass property can be applied in high electron mobility transistors (HEMTs). These materials have a low density of states (DOS) resulting a low inversion charge and drive current. Due to large lattice mismatch between III–V materials and Si, the growth of such materials on Si with high epitaxial quality is difficult. It has been reported that a GeSnSi intermediate layer will solve this problem. The lattice constant of GeSnSi can be tailored by changing the Si and Sn content in Ge and is lattice-matched to a certain III–V material. The other issues with III–V integration on Si are their high dielectric constant and inefficient surface passivation. The first issue promotes SCEs in transistors and the latter results in high gate leakage. All these points indicate that using III–V materials as channel material is challenging.

Another group of material for HEMT is AlGaN/GaN structures [65–67]. These heterostructures generate a large 2D electron gas sheet density in the range of $10^{13}\,cm^{-2}$ without doping. Some research reports have proposed GaN-based high-power amplifier transistors for future 4G telecommunication application.

AlGaN/GaN structures are grown on Si when a nucleation layer in the range of micron is grown first as a buffer layer as shown in Figure 1.36. The lattice constant of AlGaN is less than GaN and thus in a AlGaN/GaN structures, a tensile near the interface of heterojunction is created. The tensile stress generates a static charge and a polarization field is formed due to piezoelectric properties of nitrides [65]. The metal gate forms a Schottky contact on GaN (AlGaN) surface.

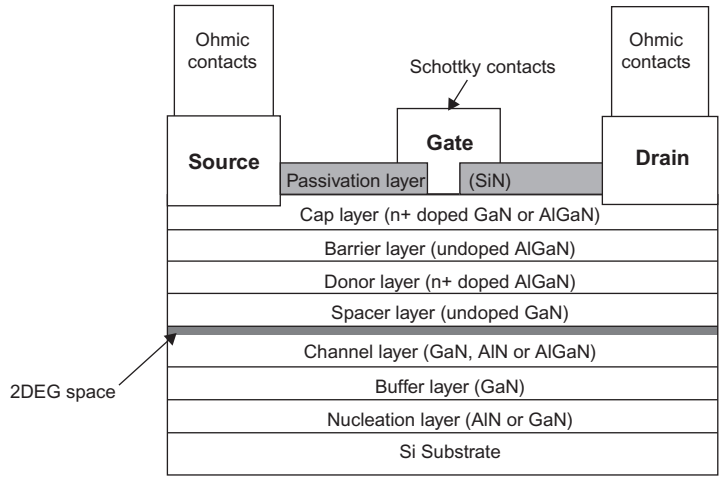

Figure 1.36 Layer structure of an AlGaN/GaN HEMT grown on Si [65–67].

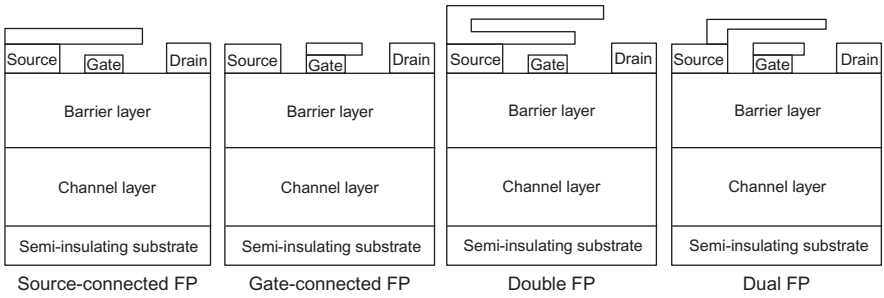

Figure 1.37 Different alternatives of field plates for GaN HEMTs [68].

Different field-plate designs have been proposed to improve the performance of the device. These methods make several features of the metallic electrodes extended over the gate and the gate–drain region [67], In this way, an electric field is established at the edge of the gate electrode from the drain side which leads to higher drain voltages and output power. A few alternatives of these methods are illustrated in Figure 1.37 [68].

Graphene Material

Graphene is a 2D crystalline structure in which carbon atoms are situated in a regular sp^2-bonded hexagonal pattern. Graphene is the building block of graphite and was for the first time isolated out of graphite in 2004 [69]. The planar structure and the ultimate thinness of

graphene give rise to outstanding mechanical, electrical, and optical properties which can be utilized in future electronic–photonic devices. These properties and some of the implementations, so far, are discussed in the coming sections.

Graphene is produced in different ways. As mentioned above, it was first extracted from graphite by a surprisingly simple but groundbreaking method called mechanical exfoliation. In this method, the layers of multilayered graphite are split step by step until a single atomic layer is achieved. Geim and Novoselov used adhesive tape to do so and therefore this method is also often called "scotch tape method." The achieved single-layer slices are then deposited on a substrate [69,70].

Epitaxy deposition can also be used to produce graphene. Epitaxy is the process of making a crystalline layer on top of a crystalline substrate. As the outstanding qualities of graphene are best attained in isolation, a substrate with minimum interaction with graphene is usually sought. Silicon carbide (SiC), metals like iridium (Ir) or hexagonal boron nitride (hBN) have been used as substrates for graphene epitaxy.

Graphene is also obtainable by low-pressure heating of SiC wafers which results in epitaxial graphene. Reduction of graphite oxide, metal–carbon melt process, slicing of carbon nanotubes, and solvent exfoliation are among the other methods to produce graphene.

Due to its 2D feature, graphene has unique electronic properties. Intrinsic and large area graphene is a gapless semiconductor or a semimetal. Figure 1.38 shows that the dispersion relation is linear (conical in 3D) for low energies near the six corners of the 2D hexagonal Brillouin zone (Dirac points). Near these six points, both electrons and

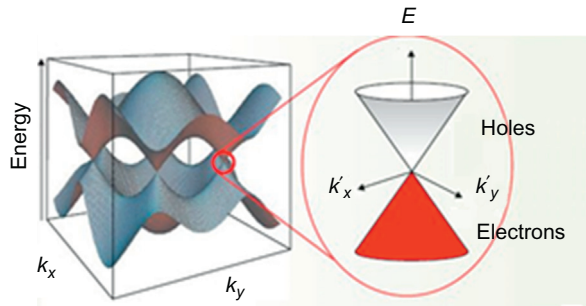

Figure 1.38 Electron energy band structure for a single-sheet graphene [71].

holes (Dirac fermions) have zero effective mass. They behave like relativistic particles described by the Dirac equation for spin-1/2 particles. The linear dispersion relation is given by

$$E = \hbar v_{\mathrm{F}} \sqrt{k_x^2 + k_y^2}$$

where v_{F} is the Fermi velocity, k_x and $k_y$are wave vectors measured from the Dirac points. The Dirac points are considered as having the zero level of energy (E).

As expected from the low charge carrier effective mass in graphene [72], transport calculations and measurements show extremely high values for electron and hole mobility: 40,000 cm^2/Vs in graphene on SiO_2 [73], 27,000 cm^2/Vs in epitaxial graphene [74], and 200,000 cm^2/Vs in suspended graphene [75]. The mobility in the latest case is limited by intrinsic acoustic phonons of graphene and is higher than that of silver in room temperature. The choice and quality of substrate for unsuspended graphene can have a great effect on graphene's mobility as scattering by phonons of the substrate is dominant comparing to the graphene intrinsic phonons. Graphene is also capable of carrying high current densities [76] and its doping is possible by donor [77] or acceptor [78] atoms. Unlike conventional metals, the density of states and Fermi energy of graphene can be tuned by electrostatic or chemical doping [79].

Graphene has interesting potencies in three main fields of application involving its electronics properties: Biosensing, radio frequency switching, and in digital logic transistors. For the first two fields, numerous successful implementations are reported, although optimization and improvement have still room to go on. The main principle of sensing by graphene employs its high sensitivity to surrounding species. Many works are based on a structure often called "graphene transistor" in which, in principle, electronic current flows in gated graphene which in turn is in contact with species to be sensed. Upon interaction, electronic current (or conductivity, noise, etc.) in the device is influenced in a way that can be characteristic of particular species (Figure 1.39).

Graphene has also been reported to be successfully used as channel in FET for radio frequency switching with outstanding cutoff frequencies. The ballistic regime in graphene which takes place at room temperature, the high intrinsic carrier mobility, and tunable input

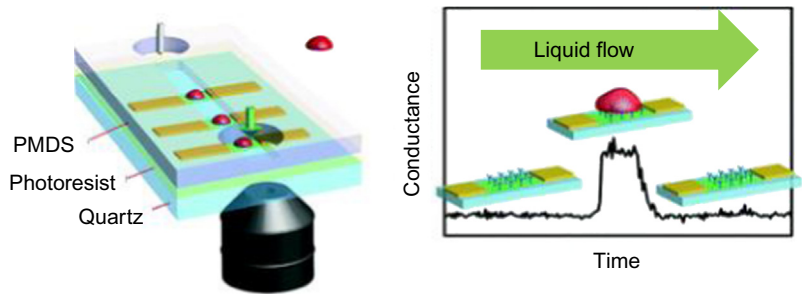

Figure 1.39 Graphene-based detection of single malaria-infected red blood cells by the changes they induce in conductivity of graphene [80].

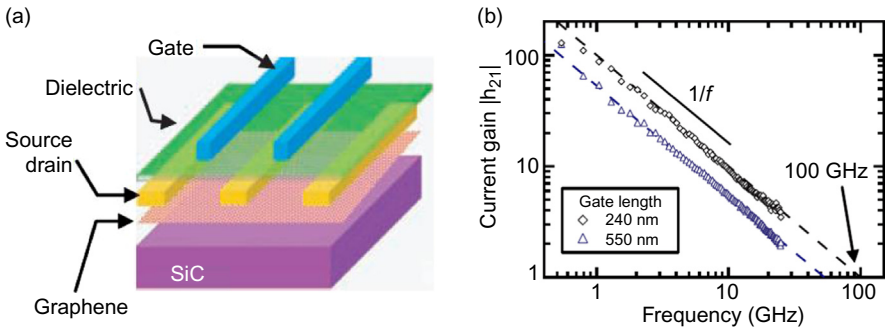

Figure 1.40 (a) Scheme of a microwave FET using graphene as its channel and (b) its current amplification gain by frequency. The cutoff frequency is ~50 and ~100 GHz for 550 and 240 nm long gates [82].

impedances around 50 Ω for graphene-based devices make it an interesting material choice for such devices [81] (Figure 1.40).

For digital logic MOSFETs, graphene's high mobility is tempting for getting very fast devices while its very small thickness can help avoiding SCEs like DIBL, threshold voltage roll-off, and impaired saturation of drain currents. It also offers higher electron velocities at high fields compared to Si or most III−V materials [83]. However, absence of a bandgap in graphene is a major obstacle that prevents simple off-switching of MOSFETs with graphene as channel material resulting in rather I_{on}/I_{off} ratios insufficient for digital logic. Therefore, more work around is required to introduce a bandgap to the design. One of the solutions is slicing the graphene into ribbons (graphene nanoribbons or GNRs). This can bring about a bandgap, but in price of dramatic decline in electron mobility. In addition, GNR processing to make perfect layers with high-quality edges is not straightforward.

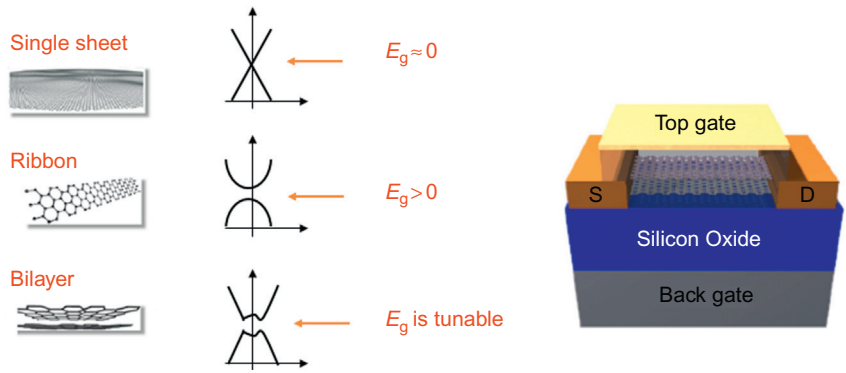

Figure 1.41 A bilayer graphene schematic and its bandgap diagram [84,87].

Another solution might be using bilayer or trilayers instead of single-layer graphene. In these structures, applying an electric field perpendicular to the layers introduces a bandgap of up to few hundred meV (Figure 1.41) [84,85]. However, the applied external electric field in turn causes a large number of carriers in the device, even in subthreshold and results in degradation of subthreshold slope [86] which represents the slope of current decline by voltage below the threshold and is important in digital logic applications.

Some other approaches to build a bandgap in graphene channeled FETs include graphene substrate interaction, lateral confinement, and straining [84], as well as introducing defects by ion irradiation [88]. Furthermore, alternative solutions by modifying the FET design (for instance by devising a physical gap along the channel [89]), totally new device concepts (like a graphene-based hot electron transistor [90]), and highly compatible gate dielectrics for graphene [91,92] have been proposed to secure high on−off current ratios with/without opening an electronic bandgap [93,94].

Silicene, Germanene, and Other Similar 2D Materials

Similar crystal structures to graphene can be thought of for other group IV elements and certain other materials. In analogy with graphene, single layers of atoms of silicon and germanium are named silicene and germanene, respectively, and are synthetically produced [95,96].

Silicene is not completely planar, as graphene is. It is buckled (Figure 1.42), meaning that some of the Si atoms are out of the plane.

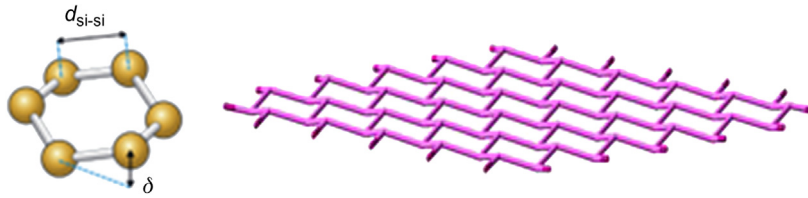

Figure 1.42 Schema of Si atoms in a hexagon of buckled silicene (left) and a typical silicene cluster with ripples on the surface (right) [97].

This formation is due to larger atomic radius of Si atom and might be utilized as it produces an electronic bandgap which graphene lacks [98]. Moreover, silicene is more compatible with silicon device technology. Dirac fermions are also predicted for silicene [99], but their existence in silicene which is deposited on metallic substrate is debated [100,101]. It is believed that the mixing of orbitals of Si atoms with metal atoms on the substrate hinder their presence. Suspended or on-insulator silicene are expected to experimentally show the Dirac fermions, but they are yet to come.

Optical properties of silicene (and germanene) are predicted to be similar to graphene with the same low-frequency absorbance in IR range [102]. Hydrogenated silicene and germanene (known as silicane or germanane, respectively) are predicted to be wide bandgap semiconductors; germanane with a direct bandgap and silicane direct or indirect, depending on its atomic configuration [103].

BN, SiC, GaN, ZnO, MnO_2 MOFs, and transition metal dichalcogenides are some other monolayer materials. "The transition metal dichalcogenides are a class of materials with the formula MX_2, where M is a transition metal element from group IV (Ti, Zr, Hf, and so on), group V (for instance, V, Nb, or Ta) or group VI (Mo, W, and so on), and X is a chalcogen (S, Se, or Te)" [104]. They possess a wide range of physical properties. In contrast to graphene, they have a sizeable electronic bandgap which can be a crucial advantage. Molybdenum disulfide (MoS_2) is one such material which is naturally available in bulk form and can be exfoliated down to monolayers. In MoS_2, similar to other transition metal dichalcogenides, each metallic (Mo) atomic layer is sandwiched between chalcogen atomic layers (sulfur). Calculations show that MoS_2 is an indirect semiconductor with a bandgap of 1.2 eV between the top of valence band (Γ point) and the

bottom of conduction band (between Γ and K points). The optical direct bandgap is situated at K point. In the monolayer, MoS_2 turns into a direct bandgap semiconductor with a gap of 1.9 eV, while the optical direct gap (at the K point) stays almost unchanged [104].

Germanium Material

Germanium is an attractive channel material for pMOSFETs due to its 4-times higher hole mobility compared to Si. The small bandgap of Ge makes higher intrinsic carrier concentration compared to Si [105] resulting in considerably higher diffusion current in Ge pn junctions. Moreover, the dielectric constant of Ge is higher than Si which makes it vulnerable to SCE and DIBL. Therefore, a transistor with Ge channel may demonstrate dominantly trap-assisted and band-to-band tunneling effects (TAT and BTBT, respectively) at high electric fields [105,106].

As examples, Ge(110) pMOSFET has shown a mobility value of 230 cm^2/Vs [107,108] (with IrO_2−$LaAlO_3$ gate dielectric) while the GOI transistors demonstrated a slightly higher mobility of ∼300 cm^2/Vs [109]. These values are, respectively, a factor of 3 and 1.5 times higher compared to universal hole mobility for Si MOSFETs on Si (110) and SOI substrates.

The carrier velocity in Ge saturates at lower electric fields in comparison with Si, therefore the Ge material is probably beneficial for the high-field operation conditions.

Inducing uniaxial strain (∼2GPa) in the channel region improves the drive current by 81%, which is 1.4 times higher compared with Si MOSFET with the same strain amount in the channel region [110].

One of the most important issues to obtain high hole mobility in germanium is the amount of defect density in the grown layers. An anisotropic surface reconstruction of Ge on Si(110) results in twins in the epitaxial layers [111].

Recently, it has been reported that GeSn alloys may have high quality and smooth layers on Ge(110) surface. These alloys have also demonstrated higher hole mobility compared to Ge [112,113]. Figure 1.43 shows a summary of the performance of Ge and GeSn alloys as channel material for pMOSFETs.

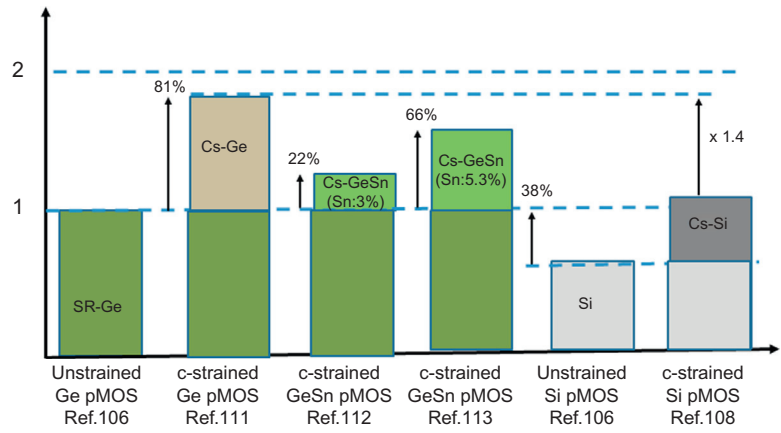

Figure 1.43 Impact of Ge and GeSn channel material (compared to Si) on the saturation drive current of a pMOSFET. The channel is strain-relaxed (SR) or compressive-strained (c-strained).

Due to large lattice constant difference between Ge and Si (4%) a high density of misfit and threading dislocations (TDs) can be generated. Different reports have demonstrated that the defect density can be reduced by post annealing treatment. For example, Lee et al has demonstrated that the TD density in a 1.5 μm thick Ge layer can be decreased from 10^8 to 10^7 after 3 min annealing at 800°C in nitrogen ambient [114].

Recent reports have demonstrated that good quality GeO_2 layers can be formed for passivation of Ge surface. The most important parameter for the quality of passivation oxide is density of interface traps (D_{it}) [traps/cm^2.eV].

A series of different oxidation methods e.g. conventional thermal oxidation [115], high-pressure oxidation [116–117], radical oxidation [118] and ozone exposure [119] have been applied to grow GeO_2. In these processes, it is important to prevent GeO_2 layer from direct contact with water moisture present in air. Therefore, the layers are capped by high-k materials [120] or rare earth oxides, e.g. Y_2O_3 [116–117].

The most common technique to deposit high-k material is atomic layer deposition (ALD). H_2O-free ALD process applying O_3 as an oxidant has been used to synthesize $HfCl_4/O_3$. The bandgap of GeO_2 bulk (H_2O assisted) is estimated to 4.3 eV and it was improved to values such as 5.4-5.9 eV for O_3-assisted grown layers.

The interface quality of GeO_2 can be improved by forming gas annealing (FGA) at 320–400 C. Higher temperatures may result in decomposition of GeO_2 layer through interaction with Ge surface. So far, D_{it} values in the range of $\sim 10^{11}\,cm^{-2}\,eV^{-1}$ have been reported for GeO_2 [115–117].

Further research for suitable gate oxides for germanium has been also done. Fluorine- or sulfur-passivated Ge surfaces have been shown as interesting ways to directly grow the high-k materials (Ge/S/Al_2O_3/HfO_2 or ZrO_2) on Ge [121–122]. Another approach for advanced gate stack for Ge MOSFETs is using rare earth oxides e.g. CeO_2 [123], La_2O_3 [124,125] or $LaLuO_3$ [116]. These oxides offer stable germanate layers and reasonable D_{it}.

Germanium is a suitable material for tunneling FETs (TFETs) due to the small bandgap. The carrier transport in TFETs occurs through tunneling of a source barrier and not diffusion over the barrier. High drive currents have been measured from Ge-TFETs which is comparable to conventional MOSFET [126].

In conclusion, there are different challenges in development of Ge-based CMOS but the on-going research activities may provide the possibilities to manufacture transistors with high performance for future industrial applications.

REFERENCES

[1] I. Ferain, C.A. Colinge, J.-P. Colinge, Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors, Nature 479 (2011) 310–316.

[2] Hall, et al., Review and perspective of high-*k* dielectrics on silicon, J. Telecommun. Inf. Technol. 2 (2007) 33–43.

[3] E.S. Yang, Microelectronic Devices, McGraw-Hill Intern. Editions, ISBN 0-07-100374-6.

[4] D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, et al., A folded-channel MOSFET for deep-sub-tenth micron era, in: IEEE International Electron Devices Meeting Technical Digest, 1998, pp. 1032–1034.

[5] S.E. Thompson, In search of forever continued transistor scaling one new material at a time, IEEE Trans. Semicond. Manuf. 18 (2005) 26.

[6] M. Jurczak, N. Collaert, A. Veloso, T. Hoffmann, S. Biesemans, Review of FINFET technology, in: 2009 IEEE International SOI Conference, Foster City, California, 2009, p. 4.

[7] G. Pei, J. Kedzierski, P. Oldiges, M. Ieong, E.C. Kan, FinFET design considerations based on 3-D simulation and analytical modeling, IEEE Trans. Electron Devices 49 (2002) 1411–1419.

[8] A. Bachtold, P. Hadley, T. Nakanishi, C. Dekker, Logic circuits with carbon nanotube transistors, Science 294 (2001) 1317–1320.

[9] J. Appenzeller, J. Knoch, V. Derycke, et al., Field-modulated carrier transport in carbon nanotube transistors, Phys. Rev. Lett. 89 (2002) 126801.

[10] A. Dixit, et al., Analysis of the parasitic S/D resistance in multiple-gate FETs, IEEE Trans. Electron Devices 52(6) (2005) 1132–1140.

[11] T. Linton, M. Chandhok, B.J. Rice, G. Schrom, Termination of the line edge roughness specification for 34 nm devices, Tech. Dig. IEDM (2002) 303.

[12] T. Yamaguchi, H. Namatsu, K. Yamazaki, K. Kurihara, Nanometer-scale linewidth fluctuations caused by polymer aggregates in resist films, Appl. Phys. Lett. 71 (1997) 2388.

[13] J. Hallstedt, P.-E. Hellstrom, H.H. Radamson, Sidewall transfer lithography for reliable fabrication of nanowires and deca-nanometer MOSFETs, Thin Solid Films 517 (2008) 117.

[14] H.H. Radamson, J. Hållstedt, Application of high-resolution x-ray diffraction for detecting defects in SiGe(C) materials, J. Phys. Condens. Matter 17 (2005) S231517.

[15] G.V. Hansson, H.H. Radamsson, W.-X. Ni, Strain and relaxation in Si-MBE structures studied by reciprocal space mapping using high resolution X-ray diffraction, J. Mater. Sci. Mater. Electron. 6 (1995) 292.

[16] P.F. Fewster, X-ray Scattering from Semiconductors, Imperial College Press, London, 2000, ISBN: 1-86094-360-8.

[17] S.P. Nikanorov, B.K. Kardashev, Elasticity and Dislocation Inelasicity of Crystals, "Nauka" Publ. House, Moscow, 1985.

[18] P. Moontragoon, Z. Ikonić, P. Harrison, Band structure calculations of Si–Ge–Sn alloys: achieving direct band gap materials, Semicond. Sci. Technol. 22 (2007) 742–748. Available from: http://dx.doi.org/10.1088/0268-1242/22/7/012.

[19] S.P. Nikanorov, Y.A. Burenkov, A.V. Stepanov, Elastic properties of silicon, Sov. Phys. Solid State 13(10) (1971) 2516–2519.

[20] H.J. McSkimin, P. Andreatch, Elastic moduli of diamond as a function of pressure and temperature, J. Appl. Phys. 43 (1972) 2944–2948.

[21] J.J. Wortman, R.A. Evans, Young's modulus, shear modulus and Poisson's ratio in silicon and germanium, J. Appl. Phys. 36 (1965) 153–156.

[22] P. Aella, C. Cook, J. Tolle, S. Zollner, A.V.G. Chizmeshya, J. Kouvetakis, Structural and optical properties of SnxSiyGe1−*x*−*y* alloys, Appl. Phys. Lett. 84 (2004) 888.

[23] J. Kouvetakis, J. Tolle, R. Roucka, V.R. D'Costa, Y.-Y. Fang, A.V.G. Chizmeshya, et al., Nanosynthesis of Si–Ge–Sn semiconductors and devices via purpose-built hydride compounds, ECS Trans. 16 (2008) 807–821. Available from: http://dx.doi.org/10.1149/1.2986840.

[24] C.W. Leitz, et al., Hole mobility enhancements and alloy scattering-limited mobility in tensile strained Si/SiGe surface channel metal–oxide–semiconductor field-effect transistors, J. Appl. Phys. 92 (2002) 3745–3751.

[25] M. Chu, Y. Sun, U. Aghoram, S.E. Thompson, Strain: a solution for higher carrier mobility in nanoscale MOSFETs, Annu. Rev. Mater. Res. 39 (2009) 203–229.

[26] A. Chaudry, G. Joshi, J.N. Roy, D.N. Singh, Review of current strained silicon nanoscaled MOSFET structures, Acta Tech. Napocensis Electron. Telecommun. 51 (2010) 15–22.

[27] S.H. Olsen, A.G. O'Neill, L.S. Driscoll, K.S.K. Kwa, S. Chattopadhyay, A.M. Waite, et al., High-performance nMOSFETs using a novel strained Si/SiGe CMOS architecture, IEEE Trans. Electron Devices 50 (2003) 1961–1969.

[28] D.J. Norris, A.G. Cullis, D.J. Paul, D.J. Robbins, High-performance nMOSFETs using a novel strained Si/SiGe CMOS architecture, IEEE Trans. Electron Devices 50 (2003) 1961–1969.

[29] S. Takagi, Understanding and engineering of carrier transport in advanced MOS channels, IEEE 52(2) (2008) 263–267.

[30] T. Mizuno, S. Takagi, N. Sugiyama, H. Satake, A. Kurobe, A. Toriumi, Electron and hole mobility enhancement in strained-Si MOSFETs on SiGe-on insulator substrates fabricated by SIMOX technology, IEEE Electron Device Lett. 21 (2000) 230–232.

[31] M.L. Lee, E.A. Fitzgerald, Optimized strained Si/strained Ge dual channel heterostructures for high mobility p- and n-MOSFETs, IEDM (2003) 18.1–4.

[32] S.E. Thompson, G. Sun, K. Wu, J. Lim, T. Nishida, Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs, in: IEDM Tech. Dig., 2004, pp. 221–224.

[33] T. Ghani, S.E. Thompson, M. Bohr, et al., A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors, in: IEDM Tech. Dig., San Francisco, CA, 2003, pp. 11.6.1–11.6.3.

[34] S. Pidin, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, et al., A novel strain enhanced CMOS architecture using selectively deposited high tensile and high compressive silicon nitride films, in: IEDM Tech. Dig., Tokyo, Japan, 2004, pp. 213–216.

[35] C.S. Smith, Piezoresistance effect in germanium and silicon, Phys. Rev. 94 (1954) 42–49.

[36] M.D. Giles, M. Armstrong, C. Auth, S.M. Cea, T. Ghani, T. Hoffman, et al., Understanding stress enhanced performance in Intel 90 nm technology, in: VLSI Symp. Tech. Dig., Honolulu, HI, 2004, pp. 118–119.

[37] J.W. Matthews, A.E. Blakeslee, Defects in epitaxial multilayers. I. Misfit dislocations, J. Cryst. Growth 27 (1974) 118.

[38] R. People, J.C. Bean, Calculation of critical layer thickness versus lattice mismatch for Ge_xSi_{1-x}/Si strained-layer heterostructures, Appl. Phys. Lett. 47, 1985, p. 229.

[39] B.W. Dodson, J.Y. Tsao, Stress dependence of dislocation glide activation energy in single-crystal silicon-germanium alloys up to 2.6 GPa, Phys. Rev. B 38 (1988) 12383.

[40] B.W. Dodson, J.Y. Tsao, Scaling relations for strained-layer relaxation, Appl. Phys. Lett. 55 (1989) 1345.

[41] H.H. Radamson, A. Bentzen, C. Menon, G. Landgren, Observed critical thickness in selectively and non-selectively grown Si1−*x*Ge*x* layers on patterned substrates, Physica Scripta, T101 (2002) 42.

[42] L. Yue, W.D. Nix, P.B. Griffin, J.D. Plummer, Critical thickness enhancement of epitaxial SiGe films grown on small structures, J. Appl. Phys. 97 (2005) 43519.

[43] T.S. Perova, J. Wasyluk, K. Lyutovich, E. Kasper, M. Oehme, K. Rode, et al., Composition and strain in thin $Si_{1-x}Ge_x$ virtual substrates measured by micro-Raman spectroscopy and x-ray diffraction, J. Appl. Phys. 109 (2011) 033502.

[44] H. Chen, Y.K. Li, C.S. Peng, H.F. Liu, Y.L. Liu, Q. Huang, et al., Crosshatching on a SiGe film grown on a Si(001) substrate studied by Raman mapping and atomic force microscopy, Phys. Rev. B 65 (2002) 233303.

[45] M.I. Alonso, K. Winer, Raman spectra of c-Si1−*x*Ge*x* alloys, Phys. Rev. B 39 (1989) 10056.

[46] J.C. Tsang, P.M. Mooney, F. Dacol, J.O. Chu, Measurements of alloy composition and strain in thin Ge*x*Si1-x layers, J. Appl. Phys. 75 (1994) 8098.

[47] J. Groenen, R. Carles, S. Christiansen, M. Albrecht, W. Dorsch, H.P. Strunk, et al., Phonons as probes in self-organized SiGe islands, Appl. Phys. Lett. 71 (1997) 3856.

[48] J. Li, A. Domenicucci, D. Chidambarrao, B. Greene, N. Rovdedo, J. Holt, et al., Stress and strain measurements in semiconductor device channel areas by convergent beam electron diffraction, Mater. Res. Soc. Symp. Proc. 913 (2006)Materials Research Society, 0913-D05-03.

[49] G.L. Wang, M. Moeen, A. Abedin, M. Kolahdouz, J. Luo, C.L. Qin, et al., Optimization of SiGe selective epitaxy for source/drain engineering in 22 nm node complementary metal–oxide semiconductor (CMOS), J. Appl. Phys. 114 (2013) 123511.

[50] J. Kouvetakis, J. Menendez, J. Tolle, Advanced Si-based semiconductors for energy and photonic applications, Diffusion and Defect Data Pt.B: Solid State Phenomena, 156–158 (2009) 77.

[51] J. Kouvetakis, J. Mathews, R. Roucka, A.V.G. Chizmeshya, J. Tolle, J. Menendez, Practical Materials Chemistry Approaches for Tuning Optical and Structural Properties of Group IV Semiconductors and Prototype Photonic Devices, IEEE Photonics J. 2 (2010) 924.

[52] O. Gurdal, P. Desjardins, J.R.A. Carlsson, N. Taylor, H.H. Radamson, J.-E. Sundgren, J.-E. Greene, Low-temperature growth and critical epitaxial thicknesses of fully strained metastable $Ge_{1-x}Sn_x$ ($x <= 0.26$) alloys on Ge(001)2×1, J. Appl. Phys. 83 (1998) 162.

[53] B. Vincent, F. Gencarelli, H. Bender, C. Merckling, B. Douhard, D.H. Petersen, O. Hensen, H.H. Henrichsen, J. Meersschaut, W. Vandervorst, M. Heyns, R. Loo, M. Caymax, Undoped and in-situ B doped GeSn epitaxial growth on Ge by atmospheric pressure-chemical vapor deposition, Appl. Phys. Lett. 99 (2011) 152103.

[54] H.H. Radamson, M. Noroozi, A. Jamshidi, M. Östling, Strain engineering in GeSnSi materials, ECS Trans. 50(9) (2013) 527.

[55] M.M. Naiini, H.H. Radamson, G.B. Malm, M. Östling, Embedded germanium PIN photodetectors in ALD slot waveguides, in: Ultimate Integration on Silicon (ULIS), 2014 15th International Conference Stockholm (2014) 45–48.

[56] M. Kolahdouz, P.T.Z. Adibi, A.A. Farniya, M. Shayestehaminzadeh, E. Trybom, L. Di Benedetto, et al., Selective growth of B- and C-doped SiGe layers in unprocessed and recessed Si openings for p-type metal–oxide–semiconductor field-effect transistors application, J. Electrochem. Soc. 157 (2010) H633.

[57] R. Loo, M. Caymax, Avoiding loading effects and facet growth key parameters for a successful implementation of selective epitaxial SiGe deposition for HBT-BiCMOS and high-mobility hetero-channel pMOS devices, Appl. Surf. Sci. 224 (2004) 24–30.

[58] S. Bodnar, E. de Berranger, P. Bouillon, M. Mouis, T. Skotnicki, J.L. Regolini, Selective Si and SiGe epitaxial heterostructures grown using an industrial low-pressure chemical vapor deposition module, J. Vac. Sci. Technol. B. Microelectron. Nanometer Struct. 15 (1997) 712.

[59] M. Kolahdouz, L. Maresca, R. Ghandi, A. Khatibi, H.H. Radamson, Kinetic model of SiGe selective epitaxial growth using RPCVD technique, J. Electrochem. Soc. 158 (2011) H457.

[60] G.L. Wang, A. Abedin, M. Moeen, M. Kolahdouz, J. Luo, T. Chen, H. H. Radamson, in press in Solid State Electronics (2014).

[61] M. Kolahdouz, L. Maresca, M. Ostling, D. Riley, R. Wise, H.H. Radamson, New method to calibrate the pattern dependency of selective epitaxy of SiGe layers, Solid State Electron. 53 (2009) 858.

[62] N. Tamura, Y. Shimamune, 45 nm CMOS technology with low temperature selective epitaxy of SiGe, Surf. Sci. 254 (2008) 6067.

[63] S. Mujumdar, K. Maitra, S. Datta, Layout-dependent strain optimization for p-channel tri-gate transistors, IEEE Trans. Electron Devices 59 (2012) 72–78.

[64] R. Chau, et al., Benchmarking nanotechnology for high-performance and low-power logic transistor applications, IEEE Trans. Nanotech. 4 (2005) 153.

[65] U.K. Mishra, P. Parikh, W. Yi-Feng, AlGaN/GaN HEMTs, an overview of device operation and applications, Proc. IEEE 90 (2002) 1022–1031.

[66] R.J. Trew, G.L. Bilbro, W. Kuang, Y. Liu, H. Yin, Microwave AlGaN/GaN HFETs, IEEE Microw. Mag. 6 (2005) 56–66.

[67] R. Chu, Z. Chen, P. Yi, S. Newman, S.P. Denbaars, U.K. Mishra, MOCVD-grown AlGaN buffer GaN HEMTs with V-gates for microwave power applications, IEEE Electron Device Lett. 30 (2009) 910–912.

[68] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, et al., Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs, IEEE Trans. Microw. Theory Tech. 31 (2010) 659–661.

[69] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, Y. Zhang, S.V. Dubonos, et al., Electric field effect in atomically thin carbon films, Science 306 (2004) 666–669.

[70] A.K. Geim, K.S. Novoselov, The rise of graphene, Nat. Mater. 6 (2007) 183–191.

[71] M. Wilson, Electron band structure in graphene. Near K and K′, the dispersion relation is relativistic with an effective mass being zer, Phys. Today (2006) 21–23.

[72] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, M.I. Katsnelson, I.V. Grigorieva, et al., Two-dimensional gas of massless Dirac fermions in graphene, Nature 438 (2005) 197–200.

[73] J.-H. Chen, C. Jang, S. Xiao, M. Ishigami, M.S. Fuhrer, Intrinsic and extrinsic performance limits of graphene devices on SiO2, Nat. Nanotechnol. 3 (2008) 206–209.

[74] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, et al., Electronic confinement and coherence in patterned epitaxial grapheme, Science 312 (2006) 1191–1196.

[75] X. Du, I. Skachko, A. Barker, E.Y. Andrei, Approaching ballistic transport in suspended graphene, Nat. Nanotechnol. 3 (2008) 491–495.

[76] J. Moser, A. Barreiro, A. Bachtold, Current-induced cleaning of graphene, Appl. Phys. Lett. 91 (2007) 163513.

[77] Y. Xue, B. Wu, L. Jiang, Y. Guo, L. Huang, J. Chen, et al., Low temperature growth of highly nitrogen-doped single crystal graphene arrays by chemical vapor deposition, J. Am. Chem. Soc. 134 (2012) 11060–11063.

[78] K.K. Kim, A. Reina, Y. Shi, H. Park, L.-J. Li, Y.H. Lee, et al., Enhancing the conductivity of transparent graphene films via doping, Nanotechnology 21 (2010) 285205.

[79] P. Avouris, S. Member, M. Freitag, Graphene photonics, plasmonics, and optoelectronics, IEEE J. Sel. Top. Quantum Electron. 20 (2014) 6000112.

[80] P.K. Ang, A. Li, M. Jaiswal, Y. Wang, H.W. Hou, J.T.L. Thong, et al., Flow sensing of single cell by graphene transistor in a microfluidic channel, Nano Lett. 11 (2011) 5240–5246.

[81] G. Deligeorgis, M. Dragoman, D. Neculoiu, D. Dragoman, G. Konstantinidis, A. Cismaru, et al., Microwave switching of graphene field effect transistor at and far from the Dirac point, Appl. Phys. Lett. 96 (2010) 103105.

[82] Y.-M. Lin, C. Dimitrakopoulos, K.A. Jenkins, D.B. Farmer, H.-Y. Chiu, A. Grill, et al., 100-GHz transistors from wafer-scale epitaxial graphene, Science 327 (2010) 662.

[83] F. Schwierz, Graphene for electronic applications—transistors and more, in: 2010 IEEE Bipolar/BiCMOS Circuits Technol. Meet., 2010, pp. 173–179.

[84] F. Xia, D.B. Farmer, Y.-M. Lin, P. Avouris, Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature, Nano Lett. 10 (2010) 715–718.

[85] E.V. Castro, K.S. Novoselov, S.V. Morozov, N.M.R. Peres, J.M.B. Lopes dos Santos, J. Nilsson, et al., Electronic properties of a biased graphene bilayer, J. Phys. Condens. Matter 22 (2010) 175503.

[86] K. Majumdar, K.V.R.M. Murali, N. Bhat, Y.-M. Lin, Intrinsic limits of subthreshold slope in biased bilayer graphene transistor, Appl. Phys. Lett. 96 (2010) 123504.

[87] C. Sealy, IBM demonstrates band gap and high on/off current in graphene FETs, Nano Today 5 (2010) 81.

[88] S. Nakaharai, T. Iijima, S. Ogawa, S.-L. Li, K. Tsukagoshi, S. Sato, et al., Current on−off operation of graphene transistor with dual gates and He ion irradiated channel, Phys. Status Solidi Vol. 10 (2013) 1608−1611.

[89] J. Hun Mun, B.J. Cho, Physical-gap-channel graphene field effect transistor with high on/off current ratio for digital logic applications, Appl. Phys. Lett. 101 (2012) 143102.

[90] S. Vaziri, G. Lupina, C. Henkel, A.D. Smith, M. Ostling, J. Dabrowski, et al., A graphene-based hot electron transistor, Nano Lett. 13 (2013) 1435−1439.

[91] W. Li, S.-L. Li, K. Komatsu, A. Aparecido-Ferreira, Y.-F. Lin, Y. Xu, et al., Realization of graphene field-effect transistor with high-κ HCa2Nb3O10 nanoflake as top-gate dielectric, Appl. Phys. Lett. 103 (2013) 023113.

[92] J. Liu, Q. Qian, Y. Zou, G. Li, Y. Jin, K. Jiang, et al., Enhanced performance of graphene transistor with ion-gel top gate, Carbon 68 (2014) 480−486.

[93] R.R. Nair, P. Blake, A.N. Grigorenko, K.S. Novoselov, T.J. Booth, T. Stauber, et al., Fine structure constant defines visual transparency of graphene, Science 320 (2008) 1308.

[94] K.F. Mak, J. Shan, T.F. Heinz, Seeing many-body effects in single- and few-layer graphene: observation of two-dimensional saddle-point excitons, Phys. Rev. Lett. 106 (2011) 046401.

[95] L. Meng, Y. Wang, L. Zhang, S. Du, R. Wu, L. Li, et al., Buckled silicene formation on Ir (111), Nano Lett. 13 (2013) 685−690.

[96] A. Fleurence, R. Friedlein, T. Ozaki, H. Kawai, Y. Wang, Y. Yamada-Takamura, Experimental evidence for epitaxial silicene on diboride thin films, Phys. Rev. Lett. 108 (2012) 245501.

[97] D. Jose, A. Datta, Structures and Chemical Properties of Silicene: Unlike Graphene, Acc. Chem. Res. 47 (2014) 59.

[98] M. Ezawa, A topological insulator and helical zero mode in silicene under an inhomogeneous electric field, New J. Phys. 14 (2012) 033003.

[99] J. Gao, J. Zhao, Initial geometries, interaction mechanism and high stability of silicene on Ag(111) surface, Sci. Rep. 2 (2012) 861.

[100] L. Chen, C.-C. Liu, B. Feng, X. He, P. Cheng, Z. Ding, et al., Evidence for Dirac fermions in a honeycomb lattice based on silicon, Phys. Rev. Lett. 109 (2012) 056804.

[101] Z.-X. Guo, S. Furuya, J. Iwata, A. Oshiyama, Absence of Dirac electrons in silicene on Ag (111) surfaces, J. Phys. Soc. Jpn. 82 (2013) 063714.

[102] F. Bechstedt, L. Matthes, P. Gori, O. Pulci, Infrared absorbance of silicene and germanene, Appl. Phys. Lett. 100 (2012) 261906.

[103] M. Houssa, E. Scalise, K. Sankaran, G. Pourtois, V.V. Afanas'ev, A. Stesmans, Electronic properties of hydrogenated silicene and germanene, Appl. Phys. Lett. 98 (2011) 223107.

[104] S. Chang, L.T.L. Lee, T. Chen, (Chapter 17: Plasmon-Enhanced Excitonic Solar Cells) in: X. Wang, Z.M. Wang (Eds.), High-Efficiency Solar Cells: Physics, Materials, and Devices, Springer International Publishing, Switzerland, 2014, pp. 515−544.

[105] E. Simoen, G. Eneman, M. Bargallo Gonzalez, D. Kobayashi, A. Luque Rodriguez, J.-A. Jiménez Tejada, et al., High Doping Density/High Electric Field, Stress and Heterojunction Effects on the Characteristics of CMOS Compatible p-n Junctions, J. Electrochem. Soc. 158 (2011) R27−R36.

[106] E. Simoen, J. Mitard, G. Hellings, G. Eneman, B. DeJaeger, L. Witters, et al., Challenges and opportunities in advanced Ge pMOSFETs, Mater. Sci. Semiconductor Process. 15 (2012) 588–600.

[107] D.S. Yu, A. Chin, C.C. Liao, C.F. Lee, C.F. Cheng, M.F. Li, et al., Three-dimensional metal gate-high-κ-GOI CMOSFETs on 1-poly-6-metal 0.18-μm Si devices, IEEE Electron. Device Lett. 26 (2005) 118–120.

[108] A. Chin, W.B. Chen, B.S. Shie, K.C. Hsu, P.C. Chen, C.H. Cheng, et al., Metal-gate/high-κ CMOS scaling from Si to Ge at small EOT, Proc. 10th Int. Conf. Solid- State Integr. Circuit Technol. (ICSICT) (The IEEE, N. Y. (2010) 978–981.

[109] S. Dissanayake, K. Tomiyama, S. Sugahara, M. Takenaka, S. Takagi, High performance ultrathin (110)-oriented Ge-on-insulator p-channel metal-oxide-semiconductor field-effect transistors fabricated by Ge condensation technique, Appl. Phys. Express 3 (2010)041302/1–3.

[110] M. Kobayashi, J. Mitard, T. Irisawa, T.-Y. Hoffmann, M. Meuris, K. Saraswat, et al., On the High-field Transport and Uniaxial Stress Effect in Ge PFETs, IEEE Trans. Electron. Dev. 58 (2011) 384–391.

[111] Y. Shimura, T. Asano, O. Nakatsuka, S. Zaima, Crystallinity improvement of epitaxial Ge grown on a Ge(110) substrate by incorporation of Sn, Appl. Phys. Express 5 (2012)015501/1–3.

[112] S. Gupta, R. Chen, B. Magyari-Kope, H. Lin, B. Yang, A. Nainani, GeSn technology: extending the Ge electronics roadmap, IEDM Tech. Dig. (IEEE, N. Y.) (2011) 398–401.

[113] G. Han, S. Su, C. Zhan, Q. Zhou, Y. Yang, L. Wang, et al., High-mobility germanium-tin (GeSn) P-channel MOSFETs featuring metallic source/drain and sub-370C process modules, IEDM Tech. Dig. (IEEE, N. Y.) (2011) 402–404.

[114] M.L. Lee, E.A. Fitzgerald, M.T. Bulsara, M.T. Currie, A. Lochtefeld, Strained Si, SiGe, and Ge channels for high-mobility metal-oxide semiconductor field-effect transistors, J. Appl. Phys. 97 (2005) 011101.

[115] A. Delabie, F. Bellenger, M. Houssa, T. Conard, S. Van Elshocht, M. Caymax, et al., Effective electrical passivation of Ge (100) for high-k gate dielectric layers using germanium oxide, Appl. Phys. Lett. 91 (2007) 141.

[116] A. Toriumi, T. Tabata, C.-H. Lee, T. Nishimura, K. Kita, K. Nagashio, Opportunities and challenges for Ge CMOS – Control of interfacing field on Ge is a key, Microelectronic Eng. 86 (2009) 1571–1576.

[117] A. Toriumi, C.H. Lee, S.K. Wang, T. Tabata, M. Yoshida, D.D. Zhao, et al., Material potential and scalability challenges of germanium CMOS, Int. Electron Devices Meeting - IEDM (2011) 28.4.1–28.4.4.

[118] M. Kobayashi, G. Thareja, M. Ishibashi, Y. Sun, P. Griffin, J. McVittie, Radical oxidation of germanium for interface gate dielectric GeO2 formation in metal-insulator-semiconductor gate stack, J. Appl. Phys. 106 (2009) 104117.

[119] D. Kuzum, J.-H. Park, T. Krishnamohan, H. S-. P. Wong, K.C. Saraswat, The effect of donor/acceptor nature of interface traps on Ge MOSFET characteristics, IEEE Trans. Electron. Devices 58 (2011) 1015–1022.

[120] M. Kobayashi, G. Thareja, M. Ishibashi, Y. Sun, P. Griffin, J. McVittie, Radical oxidation of germanium for interface gate dielectric GeO2 formation in metal-insulator-semiconductor gate stack, J. Appl. Phys. 106 (2009) 104117.

[121] D.H. Lee, H. Imajo, T. Kanashima, M. Okuyama, Improvement in the property of field effect transistor having the HfO2/Ge structure fabricated by photoassisted metal organic chemical vapor deposition with fluorine treatment, Jpn. J. Appl. Phys. 50 (2011) 04DA11.

[122] S. Sioncke, H.C. Lin, G. Brammertz, A. Delabie, T. Connard, A. Franquet, et al., S-passivation of the Ge gate stack: tuning the gate stack properties by changing the atomic layer deposition oxidant precursor, J. Electrochem. Soc. 158 (2011) H687–H692.

[123] A. Dimoulas, Y. Panaiotatos, A. Sotiropoulos, P. Tsipas, D.P. Brunco, G. Nicholas, Germanium FETs and capacitors with rare earth CeO_2/HfO_2 gates, Solid-State Electron. 51 (2007) 1508–1514.

[124] C. Henkel, S. Abermann, O. Bethge, G. Pozzovivo, P. Klang, M. Reiche, et al., Ge p-MOSFETs With Scaled ALD La_2O_3/ZrO_2 Gate Dielectrics, IEEE Trans. Electron. Devices 57 (2010) 3295–3302.

[125] C. Andersson, M.J. Suess, D.J. Webb, C. Marchiori, M. Sousa, D. Caimi, et al., Mobility and D_{it} distributions for p-channel MOSFETs with HfO_2/LaGeOx passivating layers on germanium, J. Appl. Phys. 110 (2011)114503/1–7.

[126] T. Krishnamohan, D. Kim, S. Raghunathan, K. Saraswat, Double-Gate strained Ge heterostructure tunnelingFET (TFET) with record high drive currents $\ll$60mV/dec subthreshold slope mV/dec subthreshold slope, electron devices meeting, IEDM, 2008, IEEE international electron devices meeting, IEDM (2008) 1.